CONTROL DATA® 1700
COMPUTER SYSTEM

MAINTENANCE
COMMAND TIMING CHARTS

CONTROL DATA
CORPORATION

CUSTOMER ENGINEERING MANUAL

RECORD of REVISIONS

REVISION	NOTES
A (8-19-66)	Final edition released.
B	Publication Change Order 17737, no Product Designation change. Pages 4, 7, 11, 14, 17, 19, 22, 24,
(10-17-67)	27, 29, 32, 34, 36, 37, 39, 40, 43, 45, 48, 50, 53, 55, 58, 59, 62, 65, 67, 69, 71, 72, 74 and 75 revised.
C	Manual revised; includes Engineering Change Order 20828, publication change only. Pages 1, 27,
(10-28-68)	29, 31, 32, 34, 36, 39, 40, 43, 45, 47, 48, 50, 52, 53, 55, 57, 62, 65, 66, 67, 69, 71, 74, 76,
	98, 102, 111 and 119 revised.
D	Manual revised; includes Engineering Change Order 32957. Pages 4, 8, 11, 17, 52, 58, 76,
(11-20-72)	118, 119, and 120 are revised.

FORM CA230 REV. 1-67

Pub No. 60194500

Printed in United States of America

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St. Paul, Minnesota 55112

or use Comment Sheet in the back of this manual.

COMMAND TIMING CONTENTS

COMMAND TIMING CONTENTS (cont'd)

CODE	INSTRUCTION	FUNCTION
1111=F		Addressing — Effective Address [(P+1+(P+1)]+(Q)+(00FF)

SEQUENCE / CYCLE(S):

r, Δ = 0, ind. q, i

EXECUTION TIME:

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A				
050	13	Set Δ=0	Δ = 0	
	9	Set ADR	$(F\neq 0)(\overline{\text{Sweep + Enter}})(\overline{\text{Protect Fault}})$	
	39	Clr X upper		
ADR				
A 100	51	P → Adder	(RNI)(ADR)(Δ=0)	
	49	+1 → Adder	(RNI)(ADR)(Δ=0)	
A 250	37	Set Adder → P	(RNI)(ADR)(Δ=0)	
	41	Set Adder → Y		
300	37	Adder → P		
	41	Adder → Y		
350	13	Set disable Clr r	(RNI)(ADR)(r+q) Δ = 0	
B 050	101	Req. Storage	$(\text{IM. OP.})(\overline{\text{RNI}})(\overline{\text{read index}})$	
150	9	Clr. RNI		
350	13	Clr. Disable Clr. r		
		Wait		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
		Effective Address Addressing

SEQUENCE / CYCLE(S): ind, q, i

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\Delta \neq 0 + \overline{RNI}$	
	49	Y → Adder	$(r)(\overline{RNI} + \Delta \neq 0)$ + read index	
250	41	Set Adder → Y		
300	41	Adder → Y		
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\text{read index})}$	
300	23	Clr. r	$\overline{\text{Disable Clr. r}}$	
		Wait		

CODE	INSTRUCTION	FUNCTION
		Addressing — Effective Address

SEQUENCE / CYCLE(S): ind, q, i — 3rd Pass

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	$Z \rightarrow X$		
A 100	51	$X \rightarrow$ Adder	$\Delta \neq 0 + \overline{RNI}$	
	23	Clr. ind	$(X_{15}=0)(\overline{RNI})(\overline{r})$	
250	41	Set Adder $\rightarrow$ Y		
300	41	Adder $\rightarrow$ Y		
	49	$Y \rightarrow$ Adder	$(\overline{\overline{INT}})(\overline{ind})(q)(\overline{RNI}+\Delta \neq 0)$	
	51	$Q \rightarrow$ Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta \neq 0)$	
	13	Set read index	$(\overline{INT})(\overline{ind})(i)(\overline{RNI}+\Delta \neq 0)$	
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\overline{read\ index})}$	
	39	Set Adder $\rightarrow$ X	$(\overline{ind})(q)(\overline{RNI}+\Delta \neq 0)+INT$	
	41	Set Adder $\rightarrow$ Y	$(\overline{ind})(q)(\overline{RNI}+\Delta \neq 0)(\overline{INT})$	
100	23	Clr. q	$(\overline{ind})(q)(\overline{RNI}+\Delta \neq 0)(\overline{INT})$	
100	39	Adder $\rightarrow$X		
	41	Adder $\rightarrow$ Y		
300	23	Clr. i	read index	
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): ind, q, i

EXECUTION TIME : 4th and Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\Delta \neq 0 + \overline{RNI}$	
	49	Y → Adder	$(r)(\overline{RNI} + \Delta \neq 0)$ + read index	
250	39	Set Adder → X	$(r)(\overline{RNI} + \Delta \neq 0)$ + read index	
	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index	$(\overline{INT})(\overline{ind})(i)(\overline{RNI} + \Delta \neq 0)$	
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\overline{read\ index})}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
1110 = E		Addressing: Effective Address [P+1+(P+1)] + (Q)

SEQUENCE / CYCLE(S): r, △= 0, ind, q, $\overline{i}$

EXECUTION TIME : 1st Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A				
050	13	Set △= 0	△= 0	
	9	Set ADR	(F ≠ 0)$(\overline{\text{Sweep + Enter}})(\overline{\text{Protect Fault}})$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	(RNI)(ADR)(△=0)	
	49	+1 → Adder	(RNI)(ADR)(△=0)	
A 250	37	Set Adder → P	(RNI)(ADR)(△=0)	
	41	Set Adder → Y	ADR	
300	37	Adder → P		
	41	Adder → Y		
350	13	Set Disable Clr r	(△= 0)(r + q)	
B 050	101	Req. Storage	$\overline{\text{(IM. OP.)}(\overline{\text{RNI}})(\overline{\text{read index}})}$	
150	9	Clr. RNI		
350	13	Clr. Disable Clr. r		
		Wait		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): ind, q, $\overline{i}$

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Adder	$\Delta \neq 0 + \overline{RNI}$	
	49	Y → Adder	$(r)(\overline{RNI} + \Delta \neq 0) +$ read index	
250	41	Set Adder → Y		
300	41	Adder → Y		
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\overline{\text{read index}})}$	
300	23	Clr. r	$\overline{\text{Disable Clr. r}}$	
		Wait		

CODE	INSTRUCTION	FUNCTION
		Effective Address Addressing

SEQUENCE / CYCLE(S): ind, q, $\overline{i}$

EXECUTION TIME: 3rd and Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	51	X → Adder	$\Delta \neq 0 + \overline{RNI}$	
	23	Clr. ind	$(X_{15}=0)(\overline{RNI})(\overline{r})$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	Y → Augend	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta \neq 0)$	
	51	Q → Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta \neq 0)$	
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\text{read index})}$	
	39	Set Adder → X	$(\overline{ind})(q)(\overline{RNI}+\Delta \neq 0)+INT$	
	41	Set Adder → Y	$(\overline{ind})(q)(\overline{RNI}+\Delta \neq 0)(\overline{INT})$	
100	23	Clr. q	$(\overline{ind})(q)(\overline{RNI}+\Delta \neq 0)(\overline{INT})$	
100	39	Adder → X		
	41	Adder → Y		
		Completion of timing shown on page 95.		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
1101=D		Addressing — Effective Address [P+1+(P+1)]+(00FF)

SEQUENCE / CYCLE(S): r, Δ = 0, ind, $\overline{q}$, i

EXECUTION TIME : First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A				
050	13	Set Δ = 0	Δ = 0	
	9	Set ADR	(F ≠ 0) $\overline{(\text{Sweep} + \text{Enter})}$ $\overline{(\text{Protect Fault})}$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	(RNI)(ADR)(Δ≠0)	
	49	+1 → Adder	(RNI)(ADR)(Δ≠0)	
A 250	37	Set Adder → P	(RNI)(ADR)(Δ≠0)	
	41	Set Adder → Y	ADR	
300	37	Adder → P		
	41	Adder → Y		
350	13	Set Disable Clr	r (Δ = 0)(r + q)	
B 050	101	Req. Storage	$\overline{(\text{IM. OP.})(\overline{\text{RNI}})(\overline{\text{read index}})}$	
150	9	Clr. RNI		
300		Wait		
350	13	Clr. Disable Clr. r		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
		Addressing — Effective Address

SEQUENCE / CYCLE(S): ind, $\overline{q}$, i

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\Delta \neq 0 + \overline{RNI}$	
	49	Y → Adder	$(r)(\overline{RNI} + \Delta \neq 0)$ + read index	
250	41	Set Adder → Y		
300	41	Adder → Y		
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\overline{\text{read index}})}$	
300	23	Clr. r	$\overline{\text{Disable Clr. r}}$	
		Wait		

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CODE	INSTRUCTION	FUNCTION
		Addressing — Effective Address

SEQUENCE / CYCLE(S): ind, $\overline{q}$, i

EXECUTION TIME: 3rd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	51	X → Addend	$\Delta \neq 0 + \overline{RNI}$	
	23	Clr. ind	$(X_{15}=0)(\overline{RNI})(\overline{r})$	
250	41	Set Adder → Y	$(r)(\overline{RNI}+\Delta \neq 0)$+read index	
300	41	Adder → Y		
	13	Set read index	$(\overline{INT})(\overline{ind})(i)(\overline{RNI}+\Delta \neq 0)$	
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\text{read index})}$	
300	23	Clr. i	read index	
		Wait		

CODE	INSTRUCTION	FUNCTION
		Addressing — Effective Address

SEQUENCE / CYCLE(S): ind, $\overline{q}$, i

EXECUTION TIME: 4th and Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	51	X → Adder	$\Delta \neq 0 + \overline{RNI}$	
	49	Y → Adder	$(r)(\overline{RNI} + \Delta \neq 0)$ + read index	
250	39	Set Adder → X	$(r)(\overline{RNI} + \Delta \neq 0)$ + read index	
	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index	$(\overline{INT})(\overline{ind})(i)(\overline{RNI} + \Delta \neq 0)$	
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\overline{read\ index})}$	
		Completion of timing shown on page 95.		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
1100 = C		Addressing — Effective Address [P+1+(P+1)]

SEQUENCE / CYCLE(S): r, Δ=0, ind, $\overline{q}$, $\overline{i}$ — 1st Pass

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A				
050	13	Set Δ = 0	Δ = 0	
	9	Set ADR	F ≠ (Sweep + Enter)(Protect Fault)	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	(RNI)(ADR)(Δ=0)	
	49	+1 → Adder	(RNI)(ADR)(Δ=0)	
A 250	37	Set Adder → P	(RNI)(ADR)(Δ=0)	
	41	Set Adder → Y	ADR	
300	37	Adder → P		
	41	Adder → Y		
350	13	Set Disable Clr r	(Δ = 0)(r + q)	
B 050	101	Req. Storage	(IM. OP.)(RNI)(read index)	
150	9	Clr. RNI		
300		Wait		
350	13	Clr. Disable Clr. r		

CODE	INSTRUCTION	FUNCTION
		Addressing — Effective Address

SEQUENCE / CYCLE(S): ind, $\overline{q}$, $\overline{i}$

EXECUTION TIME: 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\Delta \neq 0 + \overline{RNI}$	
	49	Y → Adder	$(r)(\overline{RNI} + \Delta \neq 0)$ + read index	
250	41	Set Adder → Y		
300	41	Adder → Y		
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\overline{\text{read index}})}$	
300	23	Clr. r	$\overline{\text{Disable Clr. r}}$	
		Wait		

CODE	INSTRUCTION	FUNCTION
		Effective Address Addressing

SEQUENCE / CYCLE(S): ind, $\overline{q}$, $\overline{i}$

EXECUTION TIME: 3rd and Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Adder	$\Delta \neq 0 + \overline{RNI}$	
	23	Clr. ind	$(X_{15}=0)(\overline{RNI})(\overline{r})$	
250	41	Set Adder → Y		
300	41	Adder → Y		
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\overline{read\ index})}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
1011 = B		Addressing — Effective Address: P+1+(P+1)+(Q)+(00FF)

SEQUENCE / CYCLE(S):

EXECUTION TIME: r, Δ = 0, $\overline{\text{ind}}$, q, i — 1st Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A				
050	13	Set Δ = 0		
	9	Set ADR	F ≠ 0 $\overline{(\text{Sweep} + \text{Enter})}$ $\overline{(\text{Protect Fault})}$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	(RNI)(ADR)(Δ=0)	
	49	+1 → Adder	(RNI)(ADR)(Δ=0)	
A 250	39	Set Adder → P	(RNI)(ADR)(Δ=0)	
	41	Set Adder → Y	ADR	
300	39	Adder → P		
	41	Adder → Y		
350	13	Set Disable Clr r	(Δ = 0)(r + q)	
B 050	101	Req. Storage	$\overline{(\text{IM. OP.})(\overline{\text{RNI}})(\text{read index})}$	
150	9	Clr. RNI		
300		Wait		
350	13	Clr. Disable Clr. r		

CODE	INSTRUCTION	FUNCTION
		Addressing — Effective Address

SEQUENCE / CYCLE(S):

EXECUTION TIME: $\overline{ind}$, q, i — 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	51	X → Addend	$\Delta \neq + \overline{RNI}$	
	49	Y → Adder	r ($\overline{RNI}$ + $\Delta \neq 0$) + read index	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	Y → Adder	($\overline{INT}$)($\overline{ind}$)(q)($\overline{RNI}$+$\Delta \neq 0$)	
	51	Q → Adder	($\overline{INT}$)($\overline{ind}$)(q)($\overline{RNI}$+$\Delta \neq 0$)	
	13	Set read index	($\overline{INT}$)($\overline{ind}$)(i)($\overline{RNI}$+$\Delta \neq 0$)	
B 050	101	Req. Storage	$\overline{(IM.\ OP.)(\overline{RNI})(\overline{read\ index})}$	
	39	Set Adder → X	($\overline{ind}$)(q)($\overline{RNI}$+$\Delta \neq 0$) + $\overline{INT}$	
	41	Set Adder → Y	($\overline{ind}$)(q)($\overline{RNI}$+ $\Delta \neq 0$) ($\overline{INT}$)	
100	23	Clr. q	($\overline{ind}$)(q)($\overline{RNI}$ + $\Delta \neq 0$)($\overline{INT}$)	
100	39	Adder → X		
	41	Adder → Y		
	23	Clr r	$\overline{\text{Disable Clr. r}}$	
300	23	Clr. i	read index	

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): $\overline{\text{ind}}$, q, i

EXECUTION TIME : 3rd and Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\Delta \neq 0 + \overline{RNI}$	
	49	Y → Adder	$(r)(\overline{RNI} + \Delta \neq 0)$+read index	
250	39	Set Adder → X	$(r)(\overline{RNI} + \Delta \neq 0)$+read index	
	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index	$(\overline{INT})(\overline{ind})(i)(\overline{RNI} + \Delta \neq 0)$	
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\overline{\text{read index}})}$	
		Completion of timing shown on page 95.		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
1010-A		Addressing — Effective Address P+1+(P+1)+(Q)

SEQUENCE / CYCLE(S): r, Δ= 0, $\overline{\text{ind}}$, q, $\overline{\text{i}}$

EXECUTION TIME: 1st Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A				
050	13	Set Δ= 0		
	9	Set ADR	F ≠ 0 $(\overline{\text{Sweep + Enter}})(\overline{\text{Protect Fault}})$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	(RNI)(ADR)(Δ=0)	
	49	+1 ↔ Adder	(RNI)(ADR)(Δ=0)	
A 250	39	Set Adder → P	(RNI)(ADR)(Δ=0)	
	41	Set Adder → Y	ADR	
300	39	Adder → P		
	41	Adder → Y		
350	13	Set Disable Clr r	(Δ= 0)(r + q)	
B 050	101	Req. Storage	$\overline{\text{(IM. OP.)}(\overline{\text{RNI}})(\overline{\text{read index}})}$	
150	9	Clr. RNI		
300		Wait		
350	13	Clr. Disable Clr. r		

CODE	INSTRUCTION	FUNCTION Addressing Effective Address

SEQUENCE / CYCLE(S): $\overline{ind}$, q, $\overline{i}$

EXECUTION TIME : 2nd and Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	51	X → Addend	$\Delta \neq 0 + \overline{RNI}$	
	49	Y → Adder	r ($\overline{RNI}$ + $\Delta \neq 0$) +	read index
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	Y → Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI} + \Delta \neq 0)$	
	51	Q → Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI} + \Delta \neq 0)$	
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(read\ index)}$	
	39	Set Adder → X	$(\overline{ind})(q)(\overline{RNI} + \Delta \neq 0) + INT$	
	41	Set Adder → Y	$(\overline{ind})(q)(\overline{RNI} + \Delta \neq 0)\ (INT)$	
100	23	Clr. q	$(\overline{ind})(q)(\overline{RNI} + \Delta \neq 0)(INT)$	
100	39	Adder → X		
	41	Adder → Y		
300	23	Clr. r	$\overline{\text{Disable Clr. r}}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
1001 = 9		Addressing: Effective Address P+1+(P+1)+(00FF)

SEQUENCE / CYCLE(S):

EXECUTION TIME: r, Δ=0, $\overline{ind}$, $\overline{q}$, i — 1st Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A				
050	13	Set Δ = 0		
	9	Set ADR	F ≠ 0 $(\overline{Sweep + Enter})(\overline{Protect\ Fault})$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	(RNI)(ADR)(Δ=0)	
	49	+1 → Adder	(RNI)(ADR)(Δ=0)	
A 250	37	Set Adder → P	(RNI)(ADR)(Δ=0)	
	41	Set Adder → Y	ADR	
300	37	Adder → P		
	41	Adder → Y		
350	13	Set Disable Clr.r	(Δ=0)(r + q)	
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\overline{read\ index})}$	
150	9	Clr. RNI		
350	13	Clr. Disable Clr. r		
		Wait		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION Addressing	Effective Address

SEQUENCE / CYCLE(S): $\overline{ind}$, $\overline{q}$, i

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	51	X → Addend	$\Delta \neq 0 + \overline{RNI}$	
	49	Y → Adder	$(r)(\overline{RNI} + \Delta \neq 0)$+read index	
250	39	Set Adder → X	$(r)(\overline{RNI} + \Delta \neq 0)$+read index	
	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Set read index	$(\overline{INT})(\overline{ind})(i)(\overline{RNI} + \Delta \neq 0)$	
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\overline{read\ index})}$	
300	23	Clr. i	read index	
	23	Clr. r	$\overline{\text{Disable clr. r}}$	
		Wait		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): $\overline{\text{ind}}$, $\overline{\text{q}}$, i

EXECUTION TIME: 3rd and Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	51	X → Addend	$\Delta \neq 0 + \overline{RNI}$	
	49	Y → Adder	$(r)(\overline{RNI} + \Delta \neq 0)$ + read index	
250	39	Set Adder → X	$(r)(\overline{RNI} + \Delta \neq 0)$ + read index	
	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index	$(\overline{INT})(\overline{ind})(i)(\overline{RNI} + \Delta \neq 0)$	
B 050	101	Req. Storage	$\overline{(IM\ .OP.)(\overline{RNI})(\text{read index})}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
1000 = 8		Addressing — Effective Address P+1+(P+1)

SEQUENCE / CYCLE(S): r, Δ= 0, $\overline{ind}$, $\overline{q}$, $\overline{i}$

EXECUTION TIME: 1st Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A				
050	13	Set Δ= 0		
	9	Set ADR	F ≠ 0 $(\overline{Sweep + Enter})(\overline{Protect\ Fault})$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	(RNI)(ADR)(Δ=0)	
	49	+1 → Adder	(RNI)(ADR)(Δ=0)	
A 250	37	Set Adder → P	(RNI)(ADR)(Δ=0)	
	41	Set Adder → Y	ADR	
300	37	Adder → P		
	41	Adder → Y		
350	13	Set Disable Clr r	(Δ= 0)(r +q)	
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(read\ index)}$	
150	9	Clr. RNI		
350	13	Clr. Disable Clr. r		
		Wait		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): $\overline{\text{ind}}$, $\overline{\text{q}}$, $\overline{\text{i}}$

EXECUTION TIME : 2nd and Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	51	X → Addend	$\Delta \neq 0 + \overline{RNI}$	
	49	Y → Adder	(r)($\overline{RNI}$+$\Delta \neq 0$)+read index	
250	41	Set Adder → Y	Unconditional	
300	41	Adder → Y		
B 050	101	Req. Storage	$\overline{\text{(IM. OP.)}(\overline{RNI})(\overline{\text{read index}})}$	
300	13	Clr. r	$\overline{\text{Disable Clr. r}}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
1111=F		Addressing: Effective Address (P+Δ)+(Q)+(00FF)

SEQUENCE / CYCLE(S): r, ind, Δ≠0, q, i

EXECUTION TIME : First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0	
	9	Set ADR	F≠0 $\overline{(\text{Sweep} + \text{Enter})}\overline{(\text{Protect Fault})}$	
	39	Clr. X upper		
	39	Extend Δ sign	r(RNI)	
ADR				
A 100	51	X → Addend	$\overline{\text{RNI}(\Delta=0)}$	
	49	Y → Adder	$r(\overline{\text{RNI}}+\Delta\neq0)$+read index	
250	39	Set Adder → X	$r(\overline{\text{RNI}}+\Delta\neq0)$+read index	
	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
B 050	101	Req. Storage	$\overline{\text{IM. OP.}(\overline{\text{RNI}})(\text{read index})}$	
150	9	Clr. RNI		
300	23	Clr. r	$\overline{\text{Disable Clr. r}}$	
		Wait for reply		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): ind, q, i

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\overline{(RNI)}(\Delta=0)$	
100	23	Clr. ind	$X_{15}=0(\overline{RNI})(\bar{r})$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	+1 → Adder	INT	
	45	Set XR	INT	
	49	Y → Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
	51	Q → Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
	13	Set read index	$ind(i)(\overline{RNI}+\Delta\neq0)(\overline{INT})$	
350	23	Clr. F	INT	
B 050	101	Req. Storage	$\overline{IM.OP.(\overline{RNI})(\overline{read\ index})}$	
	39	Set Adder → X	$(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)+INT$	
	41	Set Adder → Y	$(\overline{INT})(ind)(q)(\overline{RNI}+\Delta\neq0)$	
	41	Set state → Y	INT	
100	23	Clr. q	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
100	41	Adder → Y		
	41	state → Y		
	39	Adder → X		
300	23	Clr. i	read index	
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): i=1 (read index is set)

EXECUTION TIME : Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\overline{(RNI)(\Delta=0)}$	
	49	Y → Adder	r($\overline{RNI}$+$\Delta\neq$0)+read index	
250	41	Set Adder → Y		
250	39	Set Adder → X	r($\overline{RNI}$+$\Delta\neq$0)+read index	
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index		
B 050	101	Req. Storage	IM. OP. $\overline{(RNI)(\text{read index})}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
1110=E		Effective Address Addressing (P+Δ)+(Q)

SEQUENCE / CYCLE(S): r, ind, Δ≠0, q, $\overline{i}$

EXECUTION TIME: First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0 $\overline{(\text{Sweep} + \text{Enter})}\overline{(\text{Protect Fault})}$	
	9	Set ADR	F≠0	
	39	Clr. X upper		
	39	Extend Δ sign	(r)(RNI)	
ADR				
A 100	51	X → Addend	$\overline{(\text{RNI})(\Delta=0)}$	
	49	Y → Adder	r($\overline{\text{RNI}}$+Δ≠0)+read index	
250	39	Set Adder → X	r($\overline{\text{RNI}}$+Δ≠0)+read index	
	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
B 050	101	Req. Storage	$\overline{\text{IM. OP.}\,(\overline{\text{RNI}})(\overline{\text{read index}})}$	
150	9	Clr. RNI		
300	23	Clr. r	$\overline{\text{Disable Clr. r}}$	
		Wait for reply		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): ind=1, q=1, i=0

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	$Z \rightarrow X$		
A 100	51	$X \rightarrow$ Addend	$\overline{(RNI)(\Delta=0)}$	
100	23	Clr. ind	$X_{15}=0(\overline{RNI})\ (\overline{r})$	
250	41	Set Adder $\rightarrow$Y		
300	41	Adder $\rightarrow$ Y		
	49	+1 $\rightarrow$ Adder	INT	
	45	Set XR	INT	
	49	Y $\rightarrow$ Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
	51	Q $\rightarrow$ Adder	$(\overline{INT})(ind)(q)(\overline{RNI}+\Delta\neq0)$	
350	23	Clr. F	INT	
B 050	101	Req. Storage	$\overline{IM.OP.\ (\overline{RNI})(\overline{read\ index})}$	
	39	Set Adder $\rightarrow$X	$(\overline{ind})(\overline{q})(\overline{RNI}+\Delta\neq0)+INT$	
	41	Set Adder $\rightarrow$Y	$\overline{INT}(ind)(q)(\overline{RNI}+\Delta\neq0)$	
	41	Set state $\rightarrow$ Y	INT	
100	23	Clr. q	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
100	41	Adder $\rightarrow$Y		
	41	state $\rightarrow$ Y		
	39	Adder $\rightarrow$X		
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
1101=D		Addressing: Effective Address (P+Δ)+(00FF)

SEQUENCE / CYCLE(S): r, ind, Δ≠0, $\overline{q}$, i

EXECUTION TIME: First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0 $\overline{(\text{Sweep} + \text{Enter})}$ $\overline{(\text{Protect Fault})}$	
	9	Set ADR	F≠0	
	39	Clr. X upper		
	39	Extend Δ sign	r(RNI)	
ADR				
A 100	51	X → Addend	$\overline{(\text{RNI})(\Delta=0)}$	
	49	Y → Adder	r($\overline{\text{RNI}}$+Δ≠0)+read index	
250	39	Set Adder → X	r($\overline{\text{RNI}}$+Δ≠0)+read index	
	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
B 050	101	Req. Storage	$\overline{\text{IM. OP.}\ (\overline{\text{RNI}})(\overline{\text{read index}})}$	
150	9	Clr. RNI		
300	23	Clr. r	$\overline{\text{Disable Clr. r}}$	
		Wait for reply.		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): ind=1, q=0, i=1

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	$Z \rightarrow X$		
A 100	51	$X \rightarrow$ Addend	$\overline{(RNI)(\Delta=0)}$	
100	23	Clr. ind	$X_{15}=0(\overline{RNI})(\overline{r})$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	+1 → Adder	INT	
	45	Set XR	INT	
	13	Set read index	$\overline{ind}(i)(\overline{RNI+\Delta\neq 0})(\overline{INT})$	
350	23	Clr. F	INT	
B 050	101	Req. Storage	$\overline{IM.OP.(\overline{RNI})(\overline{read\ index})}$	
	41	Set state → Y	INT	
	39	Set Adder → X	$\overline{ind}(q)(\overline{RNI+\Delta\neq 0})\rightarrow$INT	
100	41	state → Y		
	39	Adder → X		
300	23	Clr. i	read index	
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): i=1 (read index is set) Last Pass

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\overline{(\overline{RNI})(\Delta=0)}$	
	49	Y → Adder	$r(\overline{RNI}+\Delta\neq 0)$+read index	
250	39	Set Adder → X	$r(\overline{RNI}+\Delta\neq 0)$+read index	
250	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index		
B 050	101	Req. Storage	$\overline{\text{IM. OP.}\ (\overline{RNI})(\text{read index})}$	
		Completion of timing shown on page 95.		

CODE 1100=C	INSTRUCTION	FUNCTION Effective Address Addressing (P+Δ)

SEQUENCE / CYCLE(S): r, ind, Δ≠0, $\overline{q}$, $\overline{i}$

EXECUTION TIME: First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0 $\overline{(\text{Sweep} + \text{Enter})}$ $\overline{(\text{Protect Fault})}$	
	9	Set ADR	F≠0	
	39	Clr. X upper		
	39	Extend Δ sign	r(RNI)	
ADR				
A 100	51	X → Addend	$\overline{(\text{RNI})(\Delta=0)}$	
	49	Y → Adder	r(RNI+Δ≠0)+read index	
250	39	Set Adder → X	r(RNI+Δ≠0)+read index	
	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
B 050	101	Req. Storage	$\overline{\text{IM. OP.}\ \overline{(\text{RNI})}\ \overline{(\text{read index})}}$	
150	9	Clr. RNI		
300	23	Clr. r	$\overline{\text{Disable Clr. r}}$	
		Wait for reply		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): ind=1, q=0, i=0

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	51	X → Addend	$\overline{(\overline{RNI})(\Delta=0)}$	
	23	Clr. ind	$X_{15}=0(\overline{RNI})(\overline{r})$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	+1 → Adder	INT	
	45	Set XR	INT	
350	23	Clr. F	INT	
B 050	101	Req. Storage	$\overline{IM.OP.(\overline{RNI})(\text{read index})}$	
	39	Set Adder → X	$(\overline{ind})(q)(\overline{RNI}+\Delta\neq 0)+INT$	
	41	Set state → Y	INT	
100	39	Adder → X		
	41	state → Y		
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION Effective Address
1011=B		Addressing P+Δ+(Q)+(00FF)

SEQUENCE / CYCLE(S): r, Δ≠0, $\overline{\text{ind}}$, q, i

EXECUTION TIME: First Pass

TIME		PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI					
A	000	39	Z→X		
	025	23	X→F		
	050	13	Clr. Δ=0	Δ≠0	
		9	Set ADR	F≠0 $\overline{(\text{Sweep + Enter})}$ $\overline{(\text{Protect Fault})}$	
		39	Clr. X upper		
		39	Extend Δ sign	r(RNI)	
ADR					
A	100	51	X→ Addend	$\overline{(\text{RNI})(\Delta=0)}$	
		49	Y→ Adder	r($\overline{\text{RNI}}$+Δ≠0)+read index)	
	250	39	Set Adder →X	r($\overline{\text{RNI}}$+Δ≠0)+read index	
		41	Set Adder →Y		
	300	39	Adder →X		
		41	Adder →Y		
		49	Y→ Adder	($\overline{\text{INT}}$)($\overline{\text{ind}}$)(q)($\overline{\text{RNI}}$+Δ≠0)	
		51	Q→ Adder	($\overline{\text{INT}}$)($\overline{\text{ind}}$)(q)($\overline{\text{RNI}}$+Δ≠0)	
		13	Set read index	($\overline{\text{ind}}$)(i)($\overline{\text{RNI}}$+Δ≠0)($\overline{\text{INT}}$)	
B	050	101	Req. Storage	$\overline{\text{IM. OP. }(\overline{\text{RNI}})(\overline{\text{read index}})}$	
		39	Set Adder →X	($\overline{\text{ind}}$)(q)($\overline{\text{RNI}}$+Δ≠0)+INT	
		41	Set Adder →Y	($\overline{\text{INT}}$)($\overline{\text{ind}}$)(q)($\overline{\text{RNI}}$+Δ≠0)	
	100	23	Clr. q	($\overline{\text{INT}}$)($\overline{\text{ind}}$)(q)($\overline{\text{RNI}}$+Δ≠0)	
	100	41	Adder →Y		
		39	Adder →X		
	150	9	Clr. RNI		
	300	23	Clr. r	$\overline{\text{Disable Clr. r}}$	
		23	Clr. i	read index	
			Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): i=1 (read index is set)

EXECUTION TIME : Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\overline{(RNI)(\Delta=0)}$	
	49	Y → Adder	$r(\overline{RNI}+\Delta\neq 0)$+read index	
250	39	Set Adder → X	$r(\overline{RNI}+\Delta\neq 0)$+read index	
250	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index		
B 050	101	Req. Storage	$\overline{(IM.OP.)(\overline{RNI})(\overline{\text{read index}})}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
1010=A		Addressing — Effective Address P+Δ+(Q)

SEQUENCE / CYCLE(S): r, Δ≠0, $\overline{ind}$, q, $\overline{i}$

EXECUTION TIME: First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0	
	9	Set ADR	F≠0 $\overline{(Sweep + Enter)}\overline{(Protect\ Fault)}$	
	39	Clr. X upper		
	39	Extend Δ sign	r(RNI)	
ADR				
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
	49	Y → Adder	read index+(r)($\overline{RNI}$+Δ≠0)	
250	39	Set Adder → X	read index+(r)($\overline{RNI}$+Δ≠0)	
	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	49	Y → Adder	($\overline{INT}$)($\overline{ind}$)(q)($\overline{RNI}$+Δ≠0)	
	51	Q → Adder	($\overline{INT}$)($\overline{ind}$)(q)($\overline{RNI}$+Δ≠0)	
B 050	101	Req. Storage	$\overline{IM.OP.(read\ index)(RNI)}$	
	39	Set Adder → X	($\overline{ind}$)(q)($\overline{RNI}$+Δ≠0)+INT	
	41	Set Adder → Y	(INT)($\overline{ind}$)(q)($\overline{RNI}$+Δ≠0)	
100	23	Clr. q	($\overline{INT}$)($\overline{ind}$)(q)($\overline{RNI}$+Δ≠0)	
100	41	Adder → Y		
	39	Adder → X		
300		Clr. r	$\overline{Disable\ Clr.\ r}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
1001=9		Effective Address Addressing P+Δ+(00FF)

SEQUENCE / CYCLE(S): r, Δ≠0, $\overline{\text{ind}}$, $\overline{\text{q}}$, i

EXECUTION TIME: First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0 $(\overline{\text{Sweep + Enter}})(\overline{\text{Protect Fault}})$	
	9	Set ADR	F≠0	
	39	Clr. X upper		
	39	Extend Δ sign	r(RNI)	
ADR				
A 100	51	X → Addend	$\overline{(\Delta=0)(\text{RNI})}$	
	49	Y → Adder	read index+(r)$(\overline{\text{RNI}}+\Delta\neq0)$	
250	39	Set Adder → X	read index+(r)$(\overline{\text{RNI}}+\Delta\neq0)$	
22	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Set read index	$\overline{\text{ind}}$ (i)$(\overline{\text{RNI}}+\Delta\neq0)(\overline{\text{INT}})$	
B 050	101	Req. Storage	$\overline{\text{IM. OP.}\ (\overline{\text{read index}})(\text{RNI})}$	
150	9	Clr. RNI		
300	23	Clr. r		
	23	Clr. i	read index	
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): i=1 (read index is set)

EXECUTION TIME : Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
	49	Y → Adder	read index+$r\overline{(RNI+\Delta\neq 0)}$	
250	39	Set Adder → X	read index+$r\overline{(RNI+\Delta\neq 0)}$	
250	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index		
B 050	101	Req. Storage	$\overline{IM.OP.\overline{(read\ index)}\overline{(RNI)}}$	
		Completion of timing shown on page 95.		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
1000=8	Addressing	Effective Address P+Δ

SEQUENCE / CYCLE(S): r, Δ≠0, $\overline{ind}$, $\overline{q}$, $\overline{i}$

EXECUTION TIME : First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0	
	9	Set ADR	F≠0 $(\overline{Sweep + Enter})(\overline{Protect\ Fault})$	
	39	Clr. X upper		
	39	Extend Δ sign	r(RNI)	
ADR				
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
	49	Y → Adder	read index (r)$(\overline{RNI}+\Delta\neq 0)$	
250	39	Set Adder → X	((read index +r) (RNI + Δ ≠ 0)	
	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
B 050	101	Req. Storage	$\overline{IM.\ OP.\ (\overline{read\ index})(\overline{RNI})}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
0111=7	Addressing	Effective Address (P+1)+(Q)+(00FF)

SEQUENCE / CYCLE(S):

EXECUTION TIME: $\overline{r}$, Δ=0, ind, q, i — First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Set Δ=0	Δ=0	
	9	Set ADR	F≠0 $(\overline{\text{Sweep + Enter}})(\overline{\text{Protect Fault}})$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	RNI(Δ=0)ADR.	
	49	+1 → Adder	RNI(Δ=0)ADR.	
A 250	37	Set Adder → P	RNI(Δ=0)ADR.	
	41	Set Adder → Y		
300	13	Set IM. OP.	$\overline{(r)}(\Delta=0)(\overline{\text{INT}})(\overline{\text{ind}})(i+q)(\overline{\text{STA+STQ+SPA+RAO+RTJ+JMP}})$(RNI)	
	37	Adder → P		
	41	Adder → Y		
350	13	Set Disable Clr. r	(Δ = 0)(r + q)	
B 050	101	Req. Storage	IM. OP. $\overline{(\text{read index})}\overline{(\text{RNI})}$	
150	9	Clr. RNI		
350	13	Clr. Disable Clr r		
		Wait		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION Effective Address Address

SEQUENCE / CYCLE(S): ind, q, i

EXECUTION TIME: 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
100	23	Clr. ind	$X_{15}=0(\overline{RNI})(\overline{F_{11}})$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	+1 → Adder	INT	
	45	Set XR	INT	
	49	Y → Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
	51	Q → Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
	13	Set read index	$ind(i)(\overline{RNI}+\Delta\neq0)(\overline{INT})$	
350	23	Clr. F	INT	
B 050	101	Req. Storage	$\overline{IM.OP(\overline{read\ index})(\overline{RNI})}$	
	39	Set Adder → X	$(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)+INT$	
	41	Set Adder → Y	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
	41	Set state → Y	INT	
100	23	Clr. q	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
100	41	Adder → Y		
	41	state → Y		
	39	Adder → X		
300	23	Clr. i	read index	
		Wait for reply		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): i=1 (read index is set)

EXECUTION TIME: Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
	49	Y → Adder	read index+(r)($\overline{RNI}$+$\Delta\neq0$)	
250	39	Set Adder → X	read index+(r)($\overline{RNI}$+$\Delta\neq0$)	
250	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index		
B 050	101	Req. Storage	$\overline{IM.OP.(\overline{read\ index})(\overline{RNI})}$	
		Completion of timing shown on page 95.		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
0110=6		Addressing — Effective Address (P+1)+(Q)

SEQUENCE / CYCLE(S): $\overline{r}$, Δ=0, ind, q, $\overline{i}$ — First Pass

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Set Δ=0	Δ=0	
	9	Set ADR	F≠0 $\overline{(\text{Sweep} + \text{Enter})}\overline{(\text{Protect Fault})}$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	RNI(Δ=0)ADR.	
	49	+1 → Adder	RNI(Δ=0)ADR.	
A 250	37	Set Adder → P	RNI(Δ=0)ADR.	
	41	Set Adder → Y		
300	13	Set IM. OP.	(F)(Δ=0)$(\overline{\text{INT}})(\overline{\text{ind}})(\overline{\text{i+q}})\overline{(\text{STA+STQ+SPA+RAO+RTJ+JMP})}$	
	37	Adder → P		
	41	Adder → Y		
350	13	Set Disable Clr r	(Δ = 0)(r + q)	
B 050	101	Req. Storage	IM. OP. $\overline{(\text{read index})}\overline{(\text{RNI})}$	
150	9	Clr. RNI		
300	9	Clr. ADR	RNI+ROP+STO	
350	13	Clr Disable Clr r		
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): ind=1, q=1, i=0

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
100	23	Clr. ind	$(\overline{RNI})(\overline{F_{11}})(X_{15}=0)$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	+1 → Adder	INT	
	45	Set XR	INT	
	49	Y → Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
	51	Q → Adder	$(\overline{INT})(ind)(q)(RNI+\Delta\neq0)$	
350	23	Clr. F	INT	
B 050	101	Req. Storage	$\overline{(IM.\ OP.)(\overline{read\ index})(\overline{RNI})}$	
	39	Set Adder → X	$(\overline{ind})(q)(RNI+\Delta\neq0)+INT$	
	41	Set Adder → Y	$\overline{INT}(ind)(q)(RNI+\Delta\neq0)$	
	41	Set state → Y	INT	
100	23	Clr. q	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
100	41	Adder → Y		
	41	state → Y		
	39	Adder → X		
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
0101=5	Addressing	Effective Address (P+1)+(00FF)

SEQUENCE / CYCLE(S): $\overline{r}$, Δ=0, ind, $\overline{q}$, i

EXECUTION TIME: First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
25	23	X → F		
A 050	13	Set Δ=0	Δ=0	
	9	Set ADR	F≠0 $\overline{(\text{Sweep} + \text{Enter})}\overline{(\text{Protect Fault})}$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	(Δ=0)(RNI)(ADR.	
	49	+1 → Adder	(Δ=0)(RNI)(ADR.	
A 250	37	Set Adder → P	RNI(Δ=0)(ADR.)	
	41	Set Adder → Y		
300	13	Set IM. OP.	$\overline{(R)}(\Delta=0)\overline{(INT)}\overline{(ind)}(i+q)\overline{(STA+STQ+SPA+RAO+RTJ+JMP)}$	
	37	Adder → P		
	41	Adder → Y		
350	13	Set Disable Clr r	(Δ = 0)(q + r)	
B 050	101	Req. Storage	$\overline{\text{IM. OP. } (\overline{\text{read index}})(\overline{RNI})}$	
150	9	Clr RNI		
350	13	Clr Disable Clr r		
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): ind=1, q=0, i=1

EXECUTION TIME: 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	$Z \rightarrow X$		
A 100	51	$X \rightarrow$ Addend	$\overline{(\Delta=0)(RNI)}$	
100	23	Clr. ind	$\overline{(RNI)}(X_{15}=0)\overline{(F_{11})}$	
250	41	Set Adder $\rightarrow$ Y		
300	41	Adder $\rightarrow$ Y		
	49	$+1 \rightarrow$ Adder	INT	
	45	Set XR	INT	
	13	Set read index	$\overline{ind}(i)\overline{(RNI+\Delta\neq0)}\overline{(INT)}$	
350	23	Clr. F	INT	
B 050	101	Req. Storage	$\overline{IM.OP.\overline{(read\ index)}(RNI)}$	
	41	Set state $\rightarrow$ Y	INT	
	39	Set Adder $\rightarrow$ X	$\overline{ind}(q)\overline{(RNI+\Delta\neq0)}+INT$	
100	41	state $\rightarrow$ Y		
	39	Adder $\rightarrow$ X		
300	23	Clr. i	read index	
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): i=1 (read index is set)

EXECUTION TIME : Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 00	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
	49	Y → Adder	read index+(r)$\overline{(RNI+\Delta\neq0)}$	
250	39	Set Adder → X	read index+(r)$\overline{(RNI+\Delta\neq0)}$	
250	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index		
B 050	101	Req. Storage	IM. OP. $\overline{(\text{read index})(RNI)}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
0100 = 4		Addressing — Effective Address (P+1)

SEQUENCE / CYCLE(S): $\overline{r}$, $\Delta = 0$, ind, $\overline{q}$, $\overline{i}$

EXECUTION TIME : First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Set $\Delta = 0$	$\Delta = 0$	
	9	Set ADR	$F \neq 0$ $(\overline{\text{Sweep + Enter}})(\overline{\text{Protect Fault}})$	
	39	Clr X upper		
ADR				
A 100	51	P → Adder	$(\Delta = 0)$(RNI)(ADR.)	
	49	+1 → Adder	$(\Delta = 0)$(RNI)(ADR.)	
A 250	37	Set Adder → P	$(\Delta = 0)$(RNI)(ADR.)	
	41	Set Adder → Y		
300	37	Adder → P		
	41	Adder → Y		
B 050	101	Req. Storage	IM. OP. $(\overline{\text{read index}})(\overline{\text{RNI}})$	
150	9	Clr. RNI		
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): ind=1, q=0, i=0

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	$Z \rightarrow X$		
A 100	51	$X \rightarrow$ Addend	$\overline{(\Delta=0)(\overline{RNI})}$	
	23	Clr. ind	$X_{15}=0(\overline{RNI})(\overline{F_{11}})$	
250	41	Set Adder $\rightarrow$ Y		
300	41	Adder $\rightarrow$ Y		
	49	+1 $\rightarrow$ Adder	INT	
	45	Set XR	INT	
350	23	Clr. F	INT	
B 050	101	Req. Storage	$\overline{(\underline{IM.}\ OP.)(\overline{\text{read index}})(\overline{RNI})}$	
	39	Set Adder $\rightarrow$ X	$(ind)(q)(\overline{RNI}+\Delta\neq 0)$+INT	
	41	Set state $\rightarrow$ Y	INT	
100	39	Adder $\rightarrow$ X		
	41	state $\rightarrow$ Y		
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
0011 = 3		Addressing — Effective Address (P+1)+(Q)+(00FF)

SEQUENCE / CYCLE(S):

EXECUTION TIME: $\overline{r}$, $\Delta = 0$, $\overline{ind}$, q, i — First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Set Δ = 0	Δ = 0	
	9	Set ADR	F ≠ 0 $(\overline{\text{Sweep + Enter}})(\overline{\text{Protect Fault}})$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	(Δ = 0)(RNI)(ADR.)	
	49	+1 → Adder	(Δ = 0)(RNI)(ADR.)	
A 250	37	Set Adder → P	(Δ = 0)(RNI)(ADR.)	
	41	Set Adder → Y		
300	13	Set IM. OP.	$(\overline{r})(\Delta=0)(\overline{\text{INT}})(\overline{ind})(i+q)(\overline{\text{STA+STQ+SPA+RAO+RTJ+JMP}})$	
	37	Adder → P		
	41	Adder → Y		
350	13	Set Disable Clr. r	(Δ = 0)(r + q)	
B 050	101	Req. Storage	$\overline{\text{IM. OP. } (\overline{\text{read index}})(\overline{\text{RNI}})}$	
150	9	Clr. RNI		
300		Wait		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): $\overline{r}$, $\Delta=0$, $\overline{ind}$, q, i — 2nd Pass

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	Y → Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
	51	Q → Adder	$(\overline{INT})(ind)(q)(\overline{RNI}+\Delta\neq0)$	
	13	Set read index	$(ind)(i)(\overline{RNI}+\Delta\neq0)(\overline{INT})$	
B 050	101	Req. Storage	$\overline{IM.OP.(\overline{read\ index})(\overline{RNI})}$	
	39	Set Adder → X	$(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)+INT$	
	41	Set Adder → Y	$(\overline{INT})(ind)(q)(\overline{RNI}+\Delta\neq0)$	
100	23	Clr. q	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
100	39	Adder → X		
	41	Adder → Y		
300	23	Clr. i	read index	
350	13	Clr. Disable Clr. r F/F		
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S):

i=1 (read index is set)

EXECUTION TIME : Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 00	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
	49	Y → Adder	$(r)(\overline{RNI}+\Delta\neq 0)$ + (read index)	
250	41	Set Adder → Y		
250	39	Set Adder → X	$(r)(\overline{RNI}+\Delta\neq 0)$(read index)	
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index		
B 050	101	Req. Storage	$\overline{\text{IM. OP.}\ (\overline{RNI})(\text{read index})}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
0010 = 2		Addressing — Effective Address (P+1)+(Q)

SEQUENCE / CYCLE(S): $\overline{r}$, Δ=0, $\overline{ind}$, q, $\overline{i}$

EXECUTION TIME: First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Set Δ = 0	Δ = 0	
	9	Set ADR	F ≠ 0 $(\overline{Sweep + Enter})(\overline{Protect\ Fault})$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	(RNI)(Δ=0)(ADR.)	
	49	+1 → Adder	(RNI)(Δ=0)(ADR.)	
A 250	37	Set Adder → P	(RNI)(Δ=0)(ADR.)	
	41	Set Adder → Y		
300	13	Set IM. OP.	$(RNI)(\overline{r})(\Delta = 0)(\overline{INT})(\overline{ind})(i+q)(\overline{STA+STQ+SPA+RAO+RTJ+JMP})$	
	37	Adder → P		
	41	Adder → Y		
350	13	Set Disable Clr r	$(\Delta = 0)(r + q)$	
B 050	101	Req. Storage	IM. OP. $(\overline{read\ index})(\overline{RNI})$	
150	9	Clr. RNI		
300				
350	13	Clr Disable Clr r		
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): $\overline{r}$, $\Delta=0$, $\overline{ind}$, q, $\overline{i}$

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X	(P + 1)	
A 100	51	X → Addend	$(\Delta=0)(\overline{RNI})$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	Y → Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
	51	Q → Adder	$(\overline{INT})(ind)(q)(\overline{RNI}+\Delta\neq0)$	
B 050	101	Blk. Req. Storage	$\overline{(IM.OP.)(\overline{read\ index})(\overline{RNI})}$	
	39	Set Adder → X	$(ind)(q)(\overline{RNI}+\Delta\neq0)+INT$	
	41	Set Adder → Y	$(\overline{INT})(ind)(q)(\overline{RNI}+\Delta\neq0)$	
100	23	Clr. q	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
100	39	Adder → X		
	41	Adder → Y		
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
0001=1	Addressing	Effective Address (P+1)+(00FF))

SEQUENCE / CYCLE(S): $\overline{r}$, Δ=0, $\overline{ind}$, $\overline{q}$, i

EXECUTION TIME : First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Set Δ=0	Δ=0	
	9	Set ADR	F≠0 $(\overline{\text{Sweep + Enter}})(\overline{\text{Protect Fault}})$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	(Δ=0)(RNI)(ADR)	
	49	+1 → Adder	(Δ=0)(RNI)(ADR)	
A 250	37	Set Adder → P	(Δ=0)(RNI)(ADR)	
	41	Set Adder → Y		
300	13	Set IM. OP.	$\overline{(RNI)(\overline{r})(\Delta=0)(\overline{INT})(\overline{ind})(i+q)(\overline{STA+STQ+SPA+RAO+RTJ+JMP})}$	
	37	Adder → P		
	41	Adder → Y		
B 050	101	Req. Storage	$\overline{\text{IM. OP. (read index)}}(\overline{RNI})$	
150	9	Clr. RNI		
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): $\overline{r}$, $\Delta=0$, $\overline{ind}$, $\overline{q}$, i

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	13	Set read index	$\overline{ind}(i)(\overline{RNI}+\Delta\neq 0)(\overline{INT})$	
B 050	101	Req. Storage	$\overline{IM.OP.(\overline{read\ index})(\overline{RNI})}$	
300	23	Clr. i	read index	
		Wait		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): i=1 (read index is set)

EXECUTION TIME : Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(\overline{RNI})}$	
	49	Y → Adder	$(r)(\overline{RNI}+\Delta\neq0)$+read index	
250	39	Set Adder → X	$(r)(\overline{RNI}+\Delta\neq0)$+read index	
	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index		
B 050	101	Req. Storage	$\overline{\text{IM. OP.}\,\overline{(\text{read index})}\,\overline{(RNI)}}$	
		Completion of timing shown on page 95.		

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CODE	INSTRUCTION	FUNCTION
0000 = 0		Addressing: Effective Address P+1

SEQUENCE / CYCLE(S):

EXECUTION TIME: $\overline{r}$, $\Delta = 0$, $\overline{ind}$, $\overline{q}$, $\overline{i}$ — First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Set $\Delta = 0$	$\Delta = 0$	
	9	Set ADR	$F \neq 0$ $(\overline{Sweep + Enter})(\overline{Protect\ Fault})$	
	39	Clr. X upper		
ADR				
A 100	51	P → Adder	$(\Delta=0)(RNI)(ADR)$	
	49	+1 → Adder	$(\Delta=0)(RNI)(ADR)$	
A 250	37	Set Adder → P	$(\Delta=0)(RNI)(ADR)$	
	41	Set Adder → Y		
300	37	Adder → P		
	41	Adder → Y		
B 050	101	Req. Storage	$\overline{IM.\ OP.(\overline{read\ index})(\overline{RNI})}$	
		Completion of timing shown on page 95.		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
0111=7		Effective Address Addressing (Δ)+(Q)+(00FF)

SEQUENCE / CYCLE(S): r, ind, q, i, Δ≠0

EXECUTION TIME: First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0	
	9	Set ADR	F≠0 $(\overline{\text{Sweep + Enter}})(\overline{\text{Protect Fault}})$	
	39	Clr. X upper		
ADR				
A 100	51	X → Addend	$\overline{(\Delta=0)(\text{RNI})}$	
250	41	Set Adder → Y		
300	41	Adder → Y		
B 050	101	Req. Storage	$\overline{\text{IM. OP. (read index)(RNI)}}$	
150	9	Clr. RNI		
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): ind, q, i

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 00	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
100	23	Clr. ind	$X_{15}=0(\overline{RNI})(\overline{r})$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	+1 → Adder	INT	
	45	Set XR	INT	
	49	Y → Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
	51	Q → Adder	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
	13	Set read index	$\overline{ind}(i)(\overline{RNI}+\Delta\neq0)(\overline{INT})$	
350	23	Clr. F	INT	
B 050	101	Req. Storage	$\overline{IM.OP.(\overline{read\ index})(\overline{RNI})}$	
	39	Set Adder → X	$(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)+INT$	
	41	Set Adder → Y	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
	41	Set state → Y	INT	
100	23	Clr. q	$(\overline{INT})(\overline{ind})(q)(\overline{RNI}+\Delta\neq0)$	
100	41	Adder → Y		
	41	state → Y		
	39	Adder → X		
300	23	Clr. i	read index	
		Wait for reply		

CODE	INSTRUCTION	FUNCTION
		Effective Address Addressing

SEQUENCE / CYCLE(S): i=1 (read index is set)

EXECUTION TIME : Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$(\overline{\Delta=0)(RNI})$	
	49	Y → Adder	$(r)(\overline{RNI}+\Delta\neq 0)$+read index	
250	39	Set Adder → X	$(r)(\overline{RNI}+\Delta\neq 0)$+read index	
250	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	23	Clr. read index		
B 050	101	Req. Storage	$\overline{IM.OP.(\overline{read\ index})(RNI)}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
0110=6		Addressing Effective Address (Δ)+(Q)

SEQUENCE / CYCLE(S): $\overline{r}$, ind, q, $\overline{i}$, Δ≠0

EXECUTION TIME : First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0	
	9	Set ADR	F≠0 $\overline{(\text{Sweep} + \text{Enter})}\overline{(\text{Protect Fault})}$	
	39	Clr. X upper		
ADR				
A 100	51	X → Addend	$\overline{(\Delta=0)(\text{RNI})}$	
250	41	Set Adder → Y		
300	41	Adder → Y		
B 050	101	Req. Storage	$\overline{\text{IM. OP.}\,\overline{(\text{read index})}\overline{(\text{RNI})}}$	
150	9	Clr. RNI		
		Wait		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
0101=5		Addressing — Effective Address (Δ)+(00FF)

SEQUENCE / CYCLE(S): $\overline{r}$, ind, $\overline{q}$, i, Δ≠0

EXECUTION TIME : First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0	
	9	Set ADR	F≠0 $\overline{(\text{Sweep + Enter})}$ $\overline{(\text{Protect Fault})}$	
	39	Clr. X upper		
ADR				
A 100	51	X → Addend	$\overline{(\Delta=0)(\text{RNI})}$	
250	41	Set Adder → Y		
300	41	Adder → Y		
B 050	101	Req. Storage	IM. OP. $\overline{(\text{RNI})}$ $\overline{(\text{read index})}$	
150	9	Clr. RNI		
		Wait		

CODE	INSTRUCTION	FUNCTION
		Addressing — Effective Address

SEQUENCE / CYCLE(S):

EXECUTION TIME: ind = 1, q = 1, i = 0 — 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	Z → X		
A 100	57	X → Addend	$(\overline{RNI})(\Delta = 0)$	
100	23	Clr. ind	$X_{15} = 0$ $(\overline{RNI})$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	+1 → Adder	INT	
	45	Set XR	INT	
	49	Y → Adder	(INT)(ind)(q)(RNI + $\Delta \neq 0$)	
	51	Q → Adder	(INT)(ind)(q)(RNI + $\Delta \neq 0$)	
350	23	Clr. F	INT	
B 050	101	Req. Storage	IM. OP. $(\overline{RNI})(\overline{\text{read index}})$	
	39	Set Adder → X	(ind)(q)($\overline{RNI}$ + $\Delta \neq 0$ + INT	
	41	Set Adder → Y	$\overline{INT}$ (ind)(q)($\overline{RNI}$ + $\Delta \neq 0$)	
	41	Set state → Y	INT	
100	23	Clr. q	$(\overline{INT})(\overline{ind})(q)(\overline{RNI} + \Delta \neq 0)$	
100	41	Adder → Y		
	41	state → Y		
	39	Adder → X		
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): ind=1, q=0, i=1

EXECUTION TIME : 2nd Pass

	TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR					
	000	39	$Z \rightarrow X$		
A	100	51	$X \rightarrow$ Addend	$\overline{(\Delta=0)(\overline{RNI})}$	
	100	23	Clr. ind	$X_{15}=0(\overline{RNI})(\overline{r})$	
	250	41	Set Adder $\rightarrow$ Y		
	300	41	Adder $\rightarrow$ Y		
		49	+1 $\rightarrow$ Adder	INT	
		45	Set XR	INT	
		13	Set read index	$ind(i)(\overline{\overline{RNI}+\Delta\neq 0})(\overline{INT})$	
	350	23	Clr. F	INT	
B	050	101	Req. Storage	$\overline{IM.OP.(\overline{RNI})(\overline{read\ index})}$	
		41	Set state $\rightarrow$ Y	$\overline{INT}$	
		39	Set Adder $\rightarrow$ X	$\overline{ind(q)(\overline{RNI}+\Delta\neq 0)+INT}$	
	100	41	state $\rightarrow$ Y		
		39	Adder $\rightarrow$ X		
	300	23	Clr. i	read index	
			Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): i=1 (read index is set)

EXECUTION TIME : Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(\overline{RNI})}$	
	49	Y → Adder	$(r)(\overline{RNI}+\Delta\neq 0)$+read index	
250	39	Set Adder → X	$(r)(\overline{RNI}+\Delta\neq 0)$+read index	
250	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index		
B 050	101	Req. Storage	$\overline{\text{IM. OP. } (\overline{RNI})(\overline{\text{read index}})}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
0100=4		Effective Address Addressing (Δ)

SEQUENCE / CYCLE(S): $\overline{r}$, ind, $\overline{q}$, $\overline{i}$, $\Delta \neq 0$

EXECUTION TIME : First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0	
	9	Set ADR	F≠0 $(\overline{\text{Sweep + Enter}})(\overline{\text{Protect Fault}})$	
	39	Clr. X upper		
ADR				
A 100	51	X → Addend	$\overline{(\Delta=0)(\text{RNI})}$	
250	41	Set Adder → Y		
300	41	Adder → Y		
B 050	101	Req. Storage	IM. OP. $\overline{(\text{RNI})}\overline{(\text{read index})}$	
150	9	Clr. RNI		
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): ind=1, q=0, i=0

EXECUTION TIME : 2nd Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
000	39	$Z \rightarrow X$		
A 100	51	$X \rightarrow$ Addend	$\overline{(\Delta=0)(\overline{RNI})}$	
	23	Clr. ind	$X_{15}=0(\overline{RNI})(\overline{r})$	
250	41	Set Adder $\rightarrow$ Y		
300	41	Adder $\rightarrow$ Y		
	49	+1 $\rightarrow$ Adder	INT	
	45	Set XR	INT	
350	23	Clr. F	INT	
B 050	101	Req. Storage	$\overline{IM.OP.(\overline{RNI})(\overline{read\ index})}$	
	39	Set Adder $\rightarrow$ X	$\overline{(ind)}(q)(\overline{RNI+\Delta\neq 0})$+INT	
	41	Set state $\rightarrow$ Y	INT	
100	39	Adder $\rightarrow$ X		
	41	state $\rightarrow$ Y		
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
0011=3		Addressing — Effective Address Δ+(Q)+(00FF)

SEQUENCE / CYCLE(S): $\overline{r}$, $\overline{ind}$, q, i, Δ≠0

EXECUTION TIME: First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0	
	9	Set ADR	F≠0 $(\overline{\text{Sweep + Enter}})$ $(\overline{\text{Protect Fault}})$	
	39	Clr. X upper		
ADR				
A 100	51	X → Addend	$\overline{(\Delta=0)(\text{RNI})}$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	Y → Adder	$(\overline{\text{INT}})(\overline{\text{ind}})(q)(\overline{\text{RNI}}+\Delta\neq0)$	
	51	Q → Adder	$(\overline{\text{INT}})(\overline{\text{ind}})(q)(\overline{\text{RNI}}+\Delta\neq0)$	
	13	Set read index	$(\overline{\text{ind}})(i)(\overline{\text{RNI}}+\Delta\neq0)(\overline{\text{INT}})$	
B 050	101	Req. Storage	$\overline{\text{IM. OP.}(\overline{\text{read index}})(\overline{\text{RNI}})}$	
	39	Set Adder → X	$(\overline{\text{ind}})(q)(\overline{\text{RNI}}+\Delta\neq0)+\text{INT}$	
	41	Set Adder → Y	$(\overline{\text{INT}})(\overline{\text{ind}})(q)(\overline{\text{RNI}}+\Delta\neq0)$	
100	23	Clr. q	$(\overline{\text{INT}})(\overline{\text{ind}})(q)(\overline{\text{RNI}}+\Delta\neq0)$	
100	39	Adder → X		
	41	Adder → Y		
150	9	Clr. RNI		
300	23	Clr. i	read index	
		Wait		

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): i = 1 (read index is set)

EXECUTION TIME : Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
	49	Y → Adder	$(r)(\overline{RNI}+\Delta\neq 0)$	
250	39	Set Adder → X	$(r)(\overline{RNI}+\Delta\neq 0)$	
250	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index		
B 050	101	Req. Storage	$\overline{IM.OP.(\overline{RNI})(\overline{read\ index})}$	
		Completion of timing shown on page 95.		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
0010=2		Addressing — Effective Address $\Delta+(Q)$

SEQUENCE / CYCLE(S): $\overline{r}$, $\overline{ind}$, q, $\overline{i}$, $\Delta\neq0$

EXECUTION TIME: First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0	
	9	Set ADR	F≠0 $(\overline{\text{Sweep + Enter}})(\overline{\text{Protect Fault}})$	
	39	Clr. X upper		
ADR				
A 100	51	X → Addend	$\overline{(\Delta=0)(\text{RNI})}$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	49	Y → Adder	$(\overline{\text{INT}})(\overline{\text{ind}})(q)(\overline{\text{RNI}}+\Delta\neq0)$	
	51	Q → Adder	$(\overline{\text{INT}})(\overline{\text{ind}})(q)(\overline{\text{RNI}}+\Delta\neq0)$	
B 050	101	Req. Storage	$\overline{\text{IM. OP.}(\overline{\text{RNI}})(\overline{\text{read index}})}$	
	41	Set Adder → X	$(\overline{\text{ind}})(q)(\overline{\text{RNI}}+\Delta\neq0)+\text{INT}$	
	41	Set Adder → Y	$(\overline{\text{INT}})(\overline{\text{ind}})(q)(\overline{\text{RNI}}+\Delta\neq0)$	
100	23	Clr. q	$(\overline{\text{INT}})(\overline{\text{ind}})(q)(\overline{\text{RNI}}+\Delta\neq0)$	
100	39	Adder → X		
	41	Adder → Y		
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
0001=1		Addressing — Effective Address Δ+(00FF)

SEQUENCE / CYCLE(S): $\overline{r}$, $\overline{ind}$, $\overline{q}$, i, Δ≠0

EXECUTION TIME: First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0	
	9	Set ADR	F≠0 $(\overline{\text{Sweep + Enter}})(\overline{\text{Protect Fault}})$	
	39	Clr. X upper		
ADR				
A 100	51	X → Addend	$\overline{r(\Delta=0)(RNI)}$	
250	41	Set Adder → Y		
300	41	Adder → Y		
	13	Set read index	$\overline{ind}(i)(\overline{RNI}+\Delta\neq0)(\overline{INT})$	
B 050	101	Req. Storage	$\overline{\text{IM. OP. }(\overline{RNI})(\overline{\text{read index}})}$	
150	9	Clr. RNI		
300	23	Clr. i	read index	

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION Effective Address Addressing

SEQUENCE / CYCLE(S): i=1 (read index is set)

EXECUTION TIME : Last Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 000	39	Z → X		
A 100	51	X → Addend	$\overline{(\Delta=0)(RNI)}$	
	49	Y → Adder	$(r)(\overline{RNI}+\Delta\neq 0)$+read index	
250	39	Set Adder → X	$(r)(\overline{RNI}+\Delta\neq 0)$+read index	
250	41	Set Adder → Y		
300	39	Adder → X		
	41	Adder → Y		
	13	Clr. read index		
B 050	101	Req. Storage	$\overline{IM.OP.(\overline{RNI})(\overline{\text{read index}})}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION Effective Address
0000=0		Addressing Δ

SEQUENCE / CYCLE(S): $\overline{r}, \overline{ind}, \overline{q}, \overline{i}, \Delta \neq 0$

EXECUTION TIME : First Pass

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
	23	X → F		
A 050	13	Clr. Δ=0	Δ≠0	
	9	Set ADR	F≠0 $\overline{(\text{Sweep} + \text{Enter})}\overline{(\text{Protect Fault})}$	
	39	Clr. X upper		
ADR				
A 100	51	X → Addend	$\overline{(\Delta=0)(\text{RNI})}$	
250	41	Set Adder → Y		
300	41	Adder → Y		
B 050	101	Req. Storage	$\overline{\text{IM.OP.}\overline{(\text{RNI})}\overline{(\text{read index})}}$	
		Completion of timing shown on page 95.		

CODE	INSTRUCTION	FUNCTION
SLS - 00	Selective Stop	Stop Computer If Switch is Up.

SEQUENCE / CYCLE(S): REG

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	9	Set REG	F = 0	
	39	Clr X upper		
REG				
A 300	51	P → Adder	$\overline{\text{Shift cycle}}$	Update Address for next RNI
	49	+1 → Adder	(Shift cycle)$(\overline{\text{Blk + 1}})$	
B 050	101	Req. Storage		
	41	Set Adder → Y	$\overline{\text{EXI+SPB+CPB+INT}}$	
	37	Set Adder → P	$\overline{\text{EXI+SPB+CPB}}$	
	19	Set Stop 1	(SLS)(Switch Set)$(\overline{\text{Blk. + 1}})$	
100	41	Adder → Y		
	37	Adder → P		
150	9	Set RNI	$\overline{\text{EXI+SPB+CPB+INT}}$	
325	21	Set Stop 2	Stop 1	Prevents starting Timing Chain, thereby stopping computer and giving console display. Note RNI cycle places following instruction in X before computer stops.
300	9	Clr. REG		When RUN or Step switch is pressed on console (without MC)Go 2 FF sets, causing timing and operations to continue where left off. If MC was done, RNI will be first operation.
		Wait		

CODE	INSTRUCTION	FUNCTION
Skips - 01	Skip	Skip next instruction on condition.

SEQUENCE / CYCLE(S):

REG

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	9	Set REG	F = 0	
	39	Clr X Upper		
REG				
A 100	49	X → Augend (lower 4 bits)	Skip+INQ+INP+OUT+ENQ	
	51	P → Adder	Skip+INP+OUT	
150	43	Set Skip FF	Skip condition met	
250	37	Set Adder → P	(INP+OUT)(reject)+Skip F.F.	
300	37	Adder → P		
	51	P → Adder	$\overline{\text{Shift cycle}}$	
	49	+1 → Adder	$(\overline{\text{Shift cycle}})(\overline{\text{Blk + 1}})$	
B 050	101	Req. Storage		
	37	Set Adder → P	$\overline{\text{SPB+CPB+EXI}}$	
	41	Set Adder → Y	$\overline{\text{SPB+CPB+EXI+INT}}$	Update Address for next RNI
100	37	Adder → P		
	41	Adder → Y		
150	9	Set RNI	$\overline{\text{SPB+CPB+EXI+INT}}$	
300	9	Clr. REG		

Note:

Set Adder → P indicates setting A control FF.

Adder → P indicates actual transfer.

CODE	INSTRUCTION	FUNCTION
INP-02 OUT-03	Input to A Output from A	Input, Output A

SEQUENCE / CYCLE(S):

EXECUTION TIME: REG

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	9	Set REG	F = 0	
	39	Clr. X upper		
	39	Extend sign	(REG)($\overline{\text{Skip}}$)($\overline{\text{EXI}}$)+(r)(ADR)	
REG				
A 100	49	X → Augend	Skip+INQ+INP+OUT+ENQ	
	51	P → Adder	Skip+INP+OUT	
200		Wait for reply or reject		
	19	Set Blk + 1	Internal Reject	
250	37	Set Adder → P	(INP+OUT)reject+Skip FF	REJECT sends
	31	Set I/O → A	(INP)($\overline{\text{reject}}$)	P+ Δ → P
300	37	Adder → P		
	31	I/O → A		
	51	P → Adder	$\overline{\text{Shift cycle}}$	
	49	+1 → Adder	($\overline{\text{Shift cycle}}$)($\overline{\text{Blk + 1}}$)	
B 050	101	Req. Storage		
	41	Set Adder → Y	SPB+CPB+EXI+INT	Update Address for next RNI
	37	Set Adder → P	SPB+CPB+EXI	
100	41	Adder → Y		
	37	Adder → P		
150	9	Set RNI	$\overline{\text{SPB+CPB+EXI+INT}}$	
300	9	Clr. REG		
		Wait		

CODE	INSTRUCTION	FUNCTION
EIN-04 IIN-05	Inhibit or Enable Interrupt	Inhibit or Enable Interrupt

SEQUENCE / CYCLE(S):

EXECUTION TIME: REG

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	9	Set REG	F = 0	
	39	Clr X Upper		
REG				
A 200	69	Clr. Enable INT	IIN	
A 300	51	P → Adder	$\overline{\text{Shift cycle}}$	
	49	+1 → Adder	$\overline{\text{Shift cycle}}$ ($\overline{\text{Blk + 1}}$)	
B 050	101	Req. Storage		
	37	Set Adder → P	$\overline{\text{EXI+SPB+CPB+INT}}$	Update Address for next RNI
	41	Set Adder → Y	$\overline{\text{EXI+SPB+CPB}}$	
100	41	Adder → Y		
	37	Adder → P		
150	9	Set RNI	$\overline{\text{SPB+CPB+EXI+INT}}$	
250	69	Set Enable INT	EIN+EXI	
300	9	Clr. REG		

CODE	INSTRUCTION	FUNCTION
SPB-06 CPB-07	Set or Clear Program Protect	Modify Bit 17 of word in Address (Q)

SEQUENCE / CYCLE(S):

REG

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	9	Set REG	F = 0	
	39	Clr X Upper		
REG				
A 100	51	Q → Adder	INQ+CPB+SPB+IR(X04)	
250	41	Set Adder → Y	Shift+EXI+SPB+CPB	
300	41	Adder → Y		
	51	P → Adder	$\overline{\text{Shift cycle}}$	
	49	+1 → Adder	$\overline{\text{Shift cycle}}$ ($\overline{\text{Blk+ 1}}$)	
B 050	101	Req . Storage		
	101	Set Write Prot. FF	(SPB+CPB)($\overline{\text{IM. OP}}$+RNI+read index)($\overline{\text{INT}}$)	
150	9	Set ROP	(SPB+CPB+EXI)($\overline{\text{INT}}$)	
	9	Clr. RNI		
300	9	Clr. REG		
		Wait		

CODE	INSTRUCTION	FUNCTION
SPB-06 CPB-07	Set or Clear Program Protect	

SEQUENCE / CYCLE(S): ROP

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ROP				
000	39	Z → X		
A 100	51	X → Addend		Not used
300	51	P → Adder	$\overline{EXI+MUI+DVI}$	
	44	+1 → Adder	$(\overline{EXI+MUI+DVI})$	$\overline{(Blk + 1)}$
B 050	101	Req. Storage		
	37	Set Adder → P	$\overline{RAO}$	
	41	Set Adder → Y	$\overline{RAO}$	Update Addresses for next RNI
100	37	Adder → P		
	41	Adder → Y		
150	9	Set RNI	$\overline{RAO}$	
300	9	Clr. ROP	RNI+STO	
		Wait		

CODE	INSTRUCTION	FUNCTION
IR-08	Inter-Register	Transfer and Modify data between registers.

SEQUENCE / CYCLE(S):

EXECUTION TIME : REG

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	9	Set REG	F = 0	
	39	Clr X Upper		
REG				
A 100	45	Set L.P.	IR (X07)	
	45	Set XR	IR (X06)	
	49	A → Adder	INA+IR(X05)	
	51	Q → Adder	INQ+SPB+CPB+IR(X04)	
	51	Mask → Adder	IR(X03)	
A 250	31	Set Adder → A	ENA+INA+IR(X02)	
	33	Set Adder → Q	ENQ+IR(X01)+INQ	
	71	Set Adder → Mask	IR(X00)	
275	57	Set Overflow	overflow	
300	31	Adder → A		
	33	Adder → Q		
	71	Adder → Mask		
	45	Clr. L.P.	IR	
	45	Clr. XR		
	51	P → Adder	$\overline{\text{Shift cycle}}$	Update Address for next RNI
	49	+1 → Adder	$\overline{\text{Shift cycle}}$ ($\overline{\text{Blk+ 1}}$)	
B 050	101	Req. Storage		
	41	Set Adder → Y	$\overline{\text{SPB+CPB+EXI+INT}}$	
	37	Set Adder → P	$\overline{\text{SPB+CPB+EXI}}$	
100	41	Adder → Y		
	37	Adder → P		
150	9	Set RNI	$\overline{\text{SPB+CPB+EXI+INT}}$	
300	9	Clr. REG		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
INA-09	Increase A	A + Δ W/E → A

SEQUENCE / CYCLE(S): REG

EXECUTION TIME:

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	9	Set REG	F = 0	
	39	Clr. X upper Extend sign	(REG)($\overline{\text{Skip}}$)+($\overline{\text{EXI}}$)+(RNI)(ADR)	
REG				
A 100	51	X → Addend	Shift=ENA+INA+EXI	
	49	A → Adder	INA+IR(X05)	A + Δ → Adder
250	31	Set Adder → A	INA+ENA+IR(X02)	A + Δ → A
300	31	Adder → A		
	51	P → Adder	$\overline{\text{Shift cycle}}$	
	49	+1 → Adder	$\overline{\text{Shift cycle}}$ ($\overline{\text{Blk + 1}}$)	
B 050	101	Req. Storage		
	41	Set Adder → Y	$\overline{\text{SPB+CPB+EXI+INT}}$	Update Address for next RNI
	37	Set Adder → P	$\overline{\text{SPB+CPB+EXI}}$	
100	41	Adder → Y		
	37	Adder → P		
150	9	Set RNI	$\overline{\text{SPB+CPB+EXI+INT}}$	
300	9	Clr. REG		
		Wait		

CODE	INSTRUCTION	FUNCTION
ENA-0A	Enter A	Δ to A

SEQUENCE / CYCLE(S): REG

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	9	Set REG	F = 0	
	39	Clr. X upper Extend sign	$(REG)(\overline{Skip})(\overline{EXI})+(RNI)(ADR)$	
REG				
A 100	51	X → Addend	Shift+ENA+INA+EXI	±Δ → Adder
A 250	31	Set Adder → A	ENA+INA+IR(X02)	±Δ → A
300	31	Adder → A		
	51	P → Adder	$(\overline{Shift\ cycle})$	
	49	+1 → Adder	$(\overline{Shift\ cycle})(\overline{Blk + 1})$	
B 050	101	Req. Storage		
	41	Set Adder → Y	$\overline{SPB+CPB+EXI+INT}$	Update Address for next RNI
	37	Set Adder → P	$\overline{SPB+CPB+EXI}$	
100	41	Adder → Y		
	37	Adder → P		
150	9	Set RNI	$\overline{SPB+CPB+EXI+INT}$	
300	9	Clr. REG		
		Wait		

CODE	INSTRUCTION	FUNCTION
NOP-0B	NOP Inst.	Does nothing.

SEQUENCE / CYCLE(S): REG

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
050	9	Set REG	F = 0	
	39	Clr. X upper		
REG				
A 100				
A 300	51	P → Adder	$\overline{\text{Shift cycle}}$	
	49	+1 → Adder	$\overline{\text{Shift cycle}}$ ($\overline{\text{Blk + 1}}$)	
B 050	101	Req. Storage		
	37	Set Adder → P	$\overline{\text{SPB+CPB+EXI}}$	Update Address for next RNI
	41	Set Adder → Y	$\overline{\text{SPB+CPB+EXI+INT}}$	
100	37	Adder → P		
	41	Adder → Y		
150	9	Set RNI	$\overline{\text{SPB+CPB+EXI+INT}}$	
300	9	Clr. REG		
		Wait for reply		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
ENQ-0C	Enter Q	Δ to Q

SEQUENCE / CYCLE(S): REG

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
050	39	Clr. X upper	F = 0	
	9	Set REG		
	39	Extend sign	(REG)($\overline{\text{Skip}}$)($\overline{\text{EXI}}$)+(RNI)(ADR)	
REG				
A 100	49	X → Augend	Skip+INQ+INP+OUT+ENQ	Δ → Adder
250	33	Set Adder → Q	INQ+IR(X01)+ENQ	Δ → Q
300	33	Adder → Q		
	51	P → Adder	$\overline{\text{Shift cycle}}$	
	49	+1 → Adder	$\overline{\text{Shift cycle}}$($\overline{\text{Blk + 1}}$)	
B 050	101	Req. Storage		
	37	Set Adder → P	$\overline{\text{SPB+CPB+EXI}}$	Update Address for next RNI
	41	Set Adder → Y	$\overline{\text{SPB+CPB+EXI+INT}}$	
100	37	Adder → P		
	41	Adder → Y		
150	9	Set RNI	$\overline{\text{SPB+CPB+EXI+INT}}$	
300	9	Clr. REG		
		Wait		

CODE	INSTRUCTION	FUNCTION
INQ-0D	Increase Q	Δ + Q to Q

SEQUENCE / CYCLE(S): REG

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 050	9	Set REG	F = 0	
	39	Clr. X upper Extend sign	(REG)($\overline{\text{Skip}}$)($\overline{\text{EXI}}$)+(RNI)(ADR)	
REG				
A 100	49	Set X → Augend	Skip+INQ+INP+OUT+ENQ	
	51	Q → Adder	INQ+CPB+SPB+IR(X04)	
		X → Augend		Δ + Q → Adder
250	33	Set Adder → Q	INQ+IR(X01)+ENQ	Δ + Q → Q
300	33	Adder → Q		
	51	P → Adder	($\overline{\text{Shift cycle}}$)	
	49	+1 → Adder	($\overline{\text{Shift cycle}}$)($\overline{\text{Blk+1}}$)	
B 050	101	Req. Storage		
	41	Set Adder → Y	$\overline{\text{SPB+CPB+EXI+INT}}$	Update Address for next RNI
	37	Set Adder → P	$\overline{\text{SPB+CPB+EXI}}$	
100	41	Adder → Y		
	37	Adder → P		
150	9	Set RNI	$\overline{\text{SPB+CPB+EXI+INT}}$	
300	9	Clr. REG		
		Wait		

CODE	INSTRUCTION	FUNCTION
EXI-0E	Exit Interrupt	Transfer control to (100_{16} + Δ), Enables INT, Clr./sets overflow

SEQUENCE / CYCLE(S):

REG

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X		
025	23	X → F		
A 50	9	Set REG	F = 0	
	39	Clr X Upper		
REG				
A 100	51	X → Addend	Shift+ENA+INA+EXI	
250	41	Set Adder → Y	Shift+SPB+CPB+EXI	100 + Δ → Y
300	41	Adder → Y		Delta defines the interrupt state from which the exit is taken.
	51	P → Adder	Shift cycle	
	49	+1 → Adder	Shift cycle ($\overline{\text{Blk+1}}$)	
B 050	101	Req. Storage		
150	9	Set ROP	(SPB+CPB+EXI)($\overline{\text{INT}}$)	
250	69	Set Enable INT 1	EIN+EXI	
300	9	Clr. REG		
		Wait		

CODE	INSTRUCTION	FUNCTION
EXI-0E	Exit Interrupt	

SEQUENCE / CYCLE(S): ROP

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ROP				
000	39	Z → X		
A 100	51	X → Addend		
275	57	Set overflow	$X_{15}=1$	
300	49	X → Augend	MUI(MB=1)+EXI	
B 050	101	Req. Storage		
	37	Set Adder → P	$\overline{RAO}$	
	41	Set Adder → Y	$\overline{RAO}$	
100	37	Adder → P		
	41	Adder → Y		
150	9	Set RNI	$\overline{RAO}$	
300	69	Enable INT 2		
300	9	Clr. ROP	RNI+STO	
		Wait		

CODE	INSTRUCTION	FUNCTION
0F	Shifts	

SEQUENCE / CYCLE(S): REG A

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
RNI				
000	39	Z → X'		
025	23	X → F		
A 050	9	Set REG	F = 0	
	39	Clr. X upper	$(\overline{Sweep})(\overline{ENTER})$	
	39	Extend sign	$(REG)(\overline{Skip})(\overline{EXI})+(RNI)(ADR)(r)$	
REG				
A 100	51	X → Addend	Shift+ENA+INA+EXI	
250	73	Set Shift cycle	Lower 5 bits of X ≠0	
250	41	Set Adder → Y	Shift+EXI+SPB+CPB	
300	41	Adder → Y		Y contains lower 8 bits.
	51	Q → Adder	(Shift cycle)(Q)	
	49	A → Adder	$(\text{Shift cycle})(\overline{Q})(A)$	
	45	Set L.P.	$\overline{\text{Shift cycle}}(A+Q)$	Disables Adder while shifting.
	51	P → Adder	$\overline{\text{Shift cycle}}$	} Not used unless $X_{00-04}=0$.
	49	+1 → Adder	$\overline{\text{Shift cycle}}$ (Blk-1)	
325	47	Set Shift Left	(Shift cycle)(Left)	
	47	Set Shift Right	(Shift cycle)(Right)	
350	41	Set decr. Y	$(Y_{00-04}\neq 0)$(Shift)	
	11	Set Early B cycle	$\overline{(ROP)(MUI+DVI)+\text{Shift cycle}}$	$X_{00-04}=0$
	11	Set Early C cycle	(ROP)(MUI+DVI)+Shift cycle	$X_{00-04}\neq 0$
000	11	Set B cycle	Early B set	
	11	Set C cycle	Early C set	
000	41	Decrementer → Y	Decrease Y FF set	Only the lower 5 bits of Y are decremented.

CODE	INSTRUCTION	FUNCTION
	A Shifts	

SEQUENCE / CYCLE(S): REG C

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
REG				Y is decremented twice before first shift. Thus Y = 0 when last shift is done.
C 050	31	Set Adder → A	(A → Adder)(Shift)	
	73	Clr. Shift cycle	$Y_{00-04} = 0$ ($\overline{QA}$)	
	41	Set decr. Y	$Y_{00-04} \neq 0$ ($\overline{QA}$)	
100	31	Adder → A		(A) = original quantity shifted once.
	43	decr. Y		
	49	A → Adder	Shift cycle (A)	
*250	31	Set Adder → A	(A → Adder)(Shift)	
	41	Set decr. Y	$Y_{00-04} \neq 0$	
	73	Clr. Shift cycle	$Y_{00-04} = 0$	
300	31	Adder → A		(A) = original quantity shifted twice.
	49	A → Adder	Shift cycle ($\overline{Q}$)(A)	
	7	Set H00	Shift cycle=SC 2	Stay in C cycle until $Y_{00-04} = 0$
	7	Set H06	Shift cycle=SC 2	
	51	P → Adder	Shift cycle	Start updating Address for next RNI
	49	+1 → Adder	Shift cycle	
	45	Clr. L.P.	Shift cycle	
	43	Decr. Y		
325	47	Clr. Shift Right	H06	
	47	Clr. Shift Left	H06	
000	11	Set B cycle		Allows storage to be cycled for RNI - go to page 97.

*During Short Cycle 1, 250 occurs 100 ns early.

CODE	INSTRUCTION	FUNCTION
	Q Shifts	

SEQUENCE / CYCLE(S): REG C

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
00	41	Decrementer → Y		
REG				
C 050	33	Set Adder → Q	(Q → Adder)(Shift)	
	73	Clr. Shift cycle	$Y_{00-04} = 0$ ($\overline{QA}$)	
	41	Set decr. Y	$Y_{00-04} \neq 0$ ($\overline{QA}$)	
100	33	Adder → Q	$\overline{\text{(Div Step)+(EAB)}}$	
	43	decr. Y		
	51	Q → Adder	(Shift cycle)($\overline{A}$)	
*250	33	Set Adder → Q	(Q → Adder)(Shift)	
	41	Set decr. Y	$Y_{00-04} \neq 0$	
	73	Clr. Shift cycle	$Y_{00-04} = 0$	
300	33	Adder → Q		
	51	Q → Adder	Shift cycle (Q)	
	7	Set H00	$\overline{\text{Shift cycle}}$=SC 2	
	7	H06	$\overline{\text{Shift cycle}}$=SC 2	
	51	P → Adder	$\overline{\text{Shift cycle}}$	
	49	+1 → Adder	$\overline{\text{Shift cycle}}$	
	45	Clr. L.P.	$\overline{\text{Shift cycle}}$	
325	47	Clr. Shift Right	H06	
	47	Clr. Shift Left	H06	
000	11	Set B cycle		

* During Short Cycle 1, 250 occurs 100 ns early.

CODE	INSTRUCTION	FUNCTION
	QA Shifts	

SEQUENCE / CYCLE(S):

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
	41	Decrementer →	Y	
REG				
C 050	33	Set Adder → Q	(Q → Adder)(Shift)	Q is always shifted first, then A
100	33	Adder → Q		
	57	Set Bit Bucket	$\overline{(\text{divide step})}\left[(B00)(\overline{LS})+(B15)(LS)\right]$	
	49	A → Adder	Shift cycle (A)	
	51	Clr. Q → Adder		
125	57	Set Long Shift	(ROP)(MUI+DVI)+QA Shift	
*250	31	Set Adder → A	(A → Adder)(Shift)	
	41	Set decr. Y	$Y_{00-04} \neq 0$	
	73	Clr. Shift cycle	$Y_{00-04} = 0$	
300	31	Adder → A		
	51	Q → Adder	Shift cycle (Q)	
	7	Set H00	Shift cycle	
	7	Set H06	Shift cycle	
	51	P → Adder	Shift cycle	
	49	+1 → Adder	Shift cycle	
	45	Clr. L.P.	Shift cycle	
(325)	57	Clr. Long Shift		
325	47	Clr. Shift Right		
	47	Clr. Shift Left		
000	11	Set B cycle		

* During Short Cycle 1, 250 occurs 100 ns early.

CODE	INSTRUCTION	FUNCTION
	Shifts	

SEQUENCE / CYCLE(S): REG

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
REG				
B 050	101	Req. Storage		
	41	Set Adder → Y	$\overline{SPB+CPB+EXI+INT}$	Update Address for next RNI
	37	Set Adder → P	$\overline{SPB+CPB+EXI}$	
100	41	Adder → Y		
	37	Adder → P		
150	9	Set RNI	$\overline{SPB+CPB+EXI+INT}$	
300	9	Clr. REG		
		Wait for storage resume		

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
	Any Addressing Inst.	

SEQUENCE / CYCLE(S):

EXECUTION TIME : Last of Addressing Sequence

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR 050	101	Req. Storage		
B 100	49	Y → Adder	Jump	
	49	A → Adder	STA+SPA+MUI+DVI	
	51	Q → Adder	STQ	
	51	P → Adder	INT+RTJ	
	49	X → Augend	(INT)(Δ=0)	
	49	+1 → Adder	RTJ	
	45	Set XR	EOR+(ADR)(SRI)+ROP(SRI)(MUI+DVI)	
150	9	Clear/Set RNI	(End ADR)(JMP)	End ADR = $\bar{i}$)($\overline{ind}$)($\overline{\text{read index}}$)($\overline{INT}$)
	9	Set ROP	(End ADR)($\overline{STA}$+$\overline{STQ}$+JMP+RTJ+$\overline{SPA}$)	($\overline{IM.\ OP.}$)($\overline{\text{Disable Clr.}}$ r.) +IM. OP. ($\bar{r}$)($\overline{\text{read index}}$)
	9	Set STO	INT+(End ADR)(STA+STQ+SPA+RTJ)	
200				Start of next sequence
300	9	Clr. ADR	RNI+ROP+STO	
350	7	Restart timing Chain	(ROP)(IM.OP.)	

FORM CA 206

COMMAND TIMING

CODE	INSTRUCTION	FUNCTION
JMP-1	Jump	Transfers control to (E.A.)

SEQUENCE / CYCLE(S): ADR/RNI

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
B 050	101	Req. Storage		
B 100	49	Y → Adder	Jump	Y contains effective Address upon completion of Addressing
150	9	Set RNI	(End ADR)(JMP)	
RNI				
B 250	37	Set Adder → P	(JMP)(RNI)	
B 300	37	Adder → P		effective Address in P
	9	Clr. ADR	RNI+ROP+STO	
		Wait		

CODE	INSTRUCTION	FUNCTION
MUI-2	Multiply	(E.A.) times A → QA

SEQUENCE / CYCLE(S): ROP

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
B 050	73	Set SRII	MUI(A neg) +DVI(Q neg)	
	101	Req. Storage		
B 100	49	A → Adder	MUI+DVI+SPA+STA	
	45	Set XR	(MUI+DVI)SRII	Comp. (A) if neg.
B 150	9	Set ROP	(End ADR)$\overline{(STA+STQ+SPA+RTJ+JMP)}$	
ROP				
B 250	31	Set Adder → A	(MUI+DVI)(ROP)	
300	31	Adder → A		
	9	Clr. ADR	RNI+ROP+STO	
		Wait		

CODE	INSTRUCTION	FUNCTION
MUI-2	Multiply	

SEQUENCE / CYCLE(S):

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ROP				
000	39	$Z \rightarrow X$		
A 050	41	Set $10_{16} \rightarrow Y$	MUI+DVI	Shift count → Y
100	41	$10_{16} \rightarrow Y$		Complement (E.A.) if negative. Initial signs of multiplier (A) and multiplicand (M) used in determining final sign.
	51	$X \rightarrow$ Addend	(A cycle)(ROP)	
	45	Set XR	(MUI)(M neg)+DVI (M pos)+SUB	
	73	$\overline{SR2} \rightarrow SRI$	M Pos	
	73	$SR2 \rightarrow SRI$	M Neg	
150	73	Set MB	MUI(A00=1)	Inspect bit 00 1st time only
A 250	39	Set Adder → X Set decr. Y	RAQ+SUB+MUI+DVI MUI($Y_{00-04} \neq 0$)	
	33	Clr. Q	(MUI)	
A 300	39	Adder → X		
	41	decr. Y		(Y) = 10_{16}
	51	Q → Adder	MUI+DVI	(Q) = 0-0
	49	X → Augend	((MUI)MB = 1)+EXI	(X) = multiplicand
	45	Clr. XR		
A 325	47	Set Shift Right	MUI	
A 350	11	Set Early C cycle	(ROP)(MUI+DVI)+Shift cycle	
C 000	11	Set C cycle	Early C set	

CODE	INSTRUCTION	FUNCTION
MUI-2	Multiply	

SEQUENCE / CYCLE(S):

EXECUTION TIME:

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ROP				
C 050	33	Set Adder → Q	MUI+DVI	
	73	Set Mult. step	MUI($Y_{00-04} \neq 0$)	
	73	Clr. Mult. step	($Y_{00-04} = 0$)	
100	33	Adder → Q		
	49	A → Adder	MUI+divide step	
	45	Set L. P.	MUI+DVI	
	51		Shift+Mult. step = SC1	Use Short cycle
	51		Shift+Mult. step = SC1	Use full cycle
150	31	Set Adder → A	MUI+divide step	
200	31	Adder → A		
	51	Q → Adder	MUI+DVI	
	49	Clr. A → Adder	MUI+DVI	
	45	Set XR		Use XR if ans. is to be neg.
	45	Clr. L. P.	(MUI(SRI)+DVI($Y_{00-04} = 0$)(SRII))	
225	47	Clr Right Shift FF	(MUI)	Use LP if ans. is to be pos.
*250	31	Set Adder → A	Mult. step	
	33	Set Adder → Q	MUI($\overline{\text{Mult. step}}$) +DVI	final pass only
	41	Set decr. Y	$Y_{00-04} \neq 0$	
	73	Set Mult. bit	A01 = 1	Inspect bit 01 before (A) shifted
ROP				
C 300	31	Adder → A	Adder → A set	
	33	Adder → Q	Adder → Q set	
	41	decr. Y	Decrease Y FF set	
	49	X → Augend	$\overline{\text{divide step}}$+(Mult. step)(MB = 1)	
	45	Clr. L. P.	$\overline{\text{Shift cycle}}$	
	51	Q → Adder	divide step+Mult. step	
	51	P → Adder	($\overline{\text{Shift cycle}}$)	} Start updating Address for RNI on last pass.
	49	+1 → Adder	+DVI($\overline{\text{divide step}}$) +MUI($\overline{\text{Mult. step}}$)	
	73		Mult. step	repeat C cycle
	73		$\overline{\text{Mult. step}}$	
350	11	Set Early B	$\overline{\text{Mult. step}}$	
	11	Clear Early C	$\overline{\text{Mult. step}}$	
B 000	11	Set B cycle	Early B set	
	11	Clear C cycle	Early C clear	

*During Short Cycle 1, 250 occurs 100 ns early.

CODE	INSTRUCTION	FUNCTION
MUI-2	Multiply	

SEQUENCE / CYCLE(S): ROP

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ROP				
B 050	101	Req. Storage		
	37	Set Adder → P	$\overline{RAO}$	
	41	Set Adder → Y	$\overline{RAO}$	Update Address for next RNI
100	37	Adder → P		
	41	Adder → Y		
	49	A → Adder	ADD+AND+EOR+MUI+DVI	
	45	Set XR	(MUI+DVI)SRI	Use XR if answer is to be neg.
150	9	Set RNI	$\overline{RAO}$	
250	31	Set Adder → A	MUI+DVI	
300	31	Adder → A		
	9	Clr. ROP	RNI+STO	
		Wait for reply		

CODE	INSTRUCTION	FUNCTION
DVI-3	Divide	QA divided by (E.A.) to A remainder to Q

SEQUENCE / CYCLE(S): ROP

EXECUTION TIME:

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
B 050	101 73	Req. Storage Set SR2	MUI(A neg)+DVI(Q neg)	record initial sign of dividend
B 100	49	A → Adder	MUI+DVI+SPA+STA	Comp. (A) if dividend is neg.
	45	Set XR	(MUI+DVI)SR2	
150	9	Set ROP	(End ADR)$\overline{(STA+STQ+SPA+RTJ+JMP)}$	
ROP				
B 250	31	Set Adder → A	MUI+DVI	
300	31 9	Adder → A Clr. ADR	RNI+ROP+STO	
		Wait for reply		

CODE	INSTRUCTION	FUNCTION
DVI-3	Divide	

SEQUENCE / CYCLE(S):

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ROP				
000	39	Z → X		Storage resume
A 050	41	Set 10_{16} → Y	MUI+DVI	DVI shift count → Y
100	41	10_{16} → Y		
	51	X → Addend		
	45	Set XR	(MUI)(M neg)+DVI(M pos)+SUB	
	73	$\overline{SR2}$ → SR1	M pos	Complement divisor (X) if positive.
	73	$\overline{SR2}$ → SR1	M neg	
A 250	39	Set Adder → X	RAO+SUB+MUI+DVI	
300	39	Adder → X		
	51	Q → Adder	MUI+DVI	Complement (Q) if dividend neg.
	45	Set XR	DVI(SRII)	
350	11	Set Early C FF	(ROP)(MUI+DVI)+Shift cycle	
	11	Clear Early A FF		
C 000	11	Set C cycle FF	Early C set	
	11	Clr. A cycle FF	Early A clr.	

CODE	INSTRUCTION	FUNCTION
DVI-3	Divide	

SEQUENCE / CYCLE(S):

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ROP C 050	33	Set Adder → Q	MUI+DVI	Complement (Q) if dividend neg.
100	33	Adder → Q	No EAB+$\overline{\text{divide step}}$	
	57	Set bit bucket	No EAB($\overline{\text{divide step}}$)+$\overline{\text{DIV. step}}$)($\overline{\text{LS}}$)(Bit 00)	
	49	A → Adder	MUI+divide step	Not used 1st time
	45	Set L.P.	MUI+DVI	
125	47	Set Shift Left	DVI	
	57	Set Long Shift	MUI+DVI+Shift QA	enables bit bucket → Bit 00 of A
ROP C 050	31	Set Adder → A	MUI+divide step	Not used 1st time
200	73	Set divide step	DVI($Y_{00-04} \neq 0$)	
	73	Clr. divide step	DVI($Y_{00-04} = 0$)	
200	31	Adder → A	(Adder → A FF set)	
	51	Q → Adder	MUI+DVI	
	49	Clr. A → Adder	MUI+DVI	
	45	Set XR	MUI(SR1)+DVI($Y_{00-04} = 0$)(SR2)	
	45	Clr. L.P.		
225	47	Clr. Shift Left	DVI($Y_{00-04} = 0$)	
	57	Clr. Long Shift		disconnects bit bucket from Bit 00, enables A_{15} → Bit 00.
250	33	Set Adder → Q	MUI($\overline{\text{Mult. step}}$)+DVI	
	41	Set decr. Y	$Y_{00-04} \neq 0$	
275	57	Set overflow	(DVI)($\overline{\text{divide step}}$)(A neg)	
300	45	Clr. L.P.	$\overline{\text{Shift cycle}}$	
300	33	Adder → Q		
	41	Decr. Y		
	51	Q → Adder	divide step+Mult. step	
	49	X → Augend	divide step+Mult. step (MB = 1)	
	51	P → Adder	($\overline{\text{Shift cycle}}$)	start updating Address for next RNI
	49	+1 → Adder	($\overline{\text{divide step}}$)	
			(Mult. step)	
325	47	Clr. Shift Left	DVI	
	73		$\underline{\text{divide step}}$	repeat C cycle
	73		divide step	
350	11	Set Early B		

CODE	INSTRUCTION	FUNCTION
DVI-3	Divide	

SEQUENCE / CYCLE(S):

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
B 050	101	Req. Storage		
	37	Set Adder → P	$\overline{RAO}$	
	41	Set Adder → Y	$\overline{RAO}$	Update Address for next RNI
100	37	Adder → P		
	41	Adder → Y		
	49	A → Adder	ADD+AND+EOR+MUI+DVI	
	45	Set XR	(MUI+DVI)SR1	correct final sign
150	9	Set RNI	$\overline{RAO}$	
250	31	Set Adder → A	MUI+DVI	
300	31	Adder → A		
	9	Clr. ROP	RNI+STO	
		Wait for reply		

CODE	INSTRUCTION	FUNCTION
STQ-4	Store Q	Q → (E.A.)

SEQUENCE / CYCLE(S): STO

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
B 050	101	Req. Storage		
B 100	51	Q → Adder	STQ	
B 150	9	Set STO	INT+(End ADR) (STQ+STA+SPA+RTJ)	
STO				
B 250	39	Set Adder → X		
300	9	Clr. ADR	RNI+ROP+STO	
	39	Adder → X		
		Wait		
A 000				
A 300	49	+1 → Adder		Update Address for next RNI
	51	P → Adder		
B 050	39	Req. Storage		
	37	Set Adder → P		
	41	Set Adder → Y		
100	37	Adder → P		
	41	Adder → Y		
150	9	Set RNI		
300	9	Clr. STO		

CODE	INSTRUCTION	FUNCTION
RTJ-5	Return Jump	Store P+1 in (E.A.), transfer control to (E.A.+1)

SEQUENCE / CYCLE(S): STO

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
B 050	101	Req., Storage		
B 100	51	P → Adder	INT+RTJ	
	49	+1 → Adder	RTJ	
B 150	9	Set STO	INT+(End ADR) (STQ+STA+SPA +RTJ)	
STO				
B 250	39	Set Adder → X		
300	39	Adder → X		P+1 → effective Address
	9	Clr. ADR	RNI+ROP+STO	
		Wait		
A 000				
A 100	49	Y → Adder	RTJ+INT	
A 250	37	Set Adder → P	RTJ+INT	
300	37	Adder → P		⎫
	51	P → Adder		⎪
	49	+1 → Adder		⎪
B 050	39	Req. Storage		⎪
	37	Set Adder → P		⎪ forms effective
	41	Set Adder → Y		⎪ Address+1
100	37	Adder → P		⎪
	41	Adder → Y		⎭
150	9	Set RNI		
300	9	Clr. STO		

CODE	INSTRUCTION	FUNCTION
STA-6	Store A	A to (E.A.)

SEQUENCE / CYCLE(S): STO

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
B 050	101	Req. Storage		
B 100	49	A → Adder	STA+SPA+MUI+DVI	
B 150	9	Set STO	INT+(End ADR) (STQ+STA+SPA+RTJ)	
STO				
B 250	39	Set Adder → X		
300	9	Clr. ADR	RNI+ROP+STO	
	39	Adder → X		(A) → effective Address
		Wait		
A 000				
A 100				
A 300	49	+1 → Adder		Update Address for next RNI
	51	P → Adder		
B 050	101	Req. Storage		
	37	Set Adder → P		
	41	Set Adder → Y		
100	37	Adder → P		
	41	Adder → Y		
150	9	Set RNI		
300	9	Clr. STO		

CODE	INSTRUCTION	FUNCTION
SPA-7	Store, Parity to A	A → (E.A.) Parity bit → A

SEQUENCE / CYCLE(S): STO

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
B 050	101	Req. Storage		
B 100	49	A → Adder	STA+SPA+MUI+DVI	
B 150	9	Set STO	INT+(End ADR) (STQ+STA+SPA+RTJ)	
STO				
B 250	39	Set Adder → X		
300	9	Clr. ADR	RNI+ROP+STO	
	39	Adder → X		(A) → effective Address
		Wait		
A 100	49	+1 → Adder	SPA($\overline{\text{write Aborted}}$)	
A 250	31	Set Adder → A	(SPA)($\overline{\text{Write Aborted}}$)(Parity of A Even)	
	11	Clr. A	SPA($\overline{\text{Write Aborted}}$)	
300	31	Adder → A		Parity bit → A
	49	+1 → Adder		
	51	P → Adder		
B 050	101	Req. Storage		
	37	Set Adder → P		
	41	Set Adder → Y		Update Address for next RNI
100	37	Adder → P		
	41	Adder → Y		
150	9	Set RNI		
300	9	Clr. STO		

CODE	INSTRUCTION	FUNCTION
ADD=8	Add to A	A + (E.A.) to A

SEQUENCE / CYCLE(S): ROP

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
B 050	101	Req. Storage		
B 150	9	Set ROP 1	(End ADR)($\overline{\text{STA+JMP+STQ+SPA+RTJ}}$)	
B 300	9	Clr. ADR	RNI+ROP+STO	
		Wait for reply		
A 000	39	Z → X		
ROP				
A 100	51	X → Addend		Not used - cleared at time 300
A 300	49	+1 → Adder	($\overline{\text{EXI}}$)($\overline{\text{MUI}}$)($\overline{\text{DVI}}$)	
	51	P → Adder	($\overline{\text{EXI}}$)($\overline{\text{MUI}}$)($\overline{\text{DVI}}$)	
B 050	101	Req. Storage		
	37	Set Adder → P	$\overline{\text{RAO}}$	
	41	Set Adder → Y	$\overline{\text{RAO}}$	Update Address for next RNI
100	37	Adder → P		
	41	Adder → Y		
	51	X → Addend	($\overline{\text{ADQ}}$)($\overline{\text{MUI}}$)($\overline{\text{DVI}}$)	
	49	A → Adder	ADD+AND+EOR+SUB+DVI+MUI	
150	9	Set RNI	$\overline{\text{RAO}}$	
RNI				
B 250	31	Set Adder → A	(LDA+ADD+AND+EOR+SUB)(RNI)	
300	31	Adder → A		A + (E.A.) → A
	9	Clr. ROP	RNI+STO	
		Wait for reply		

CODE	INSTRUCTION	FUNCTION
SUB-9	Subtract from A	A - (E. A.) to A

SEQUENCE / CYCLE(S): ROP

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
B 050	101	Req. Storage		
B 150	9	Set ROP	(End ADR)(STA+JMP+SQA+SPA+RTJ)	
B 300	9	Clr. ADR	RNI+ROP+STO	
		Wait for reply		
A 000	39	Z → X		
ROP				
A 100	51	X → Addend		Causes (X) to be complemented, thereby, allowing a difference of (A) and (E. A.) to be formed.
	45	Set XR or		
			MUI(M neg)+DVI(M pos)+SUB	
A 250	39	Set Adder → X	SUB+DVI+MUI	
300	39	Adder → X		
	49	+1 → Adder	$\overline{EXI}(\overline{MUI})(\overline{DVI})$	
	51	P → Adder	$\overline{EXI}(\overline{MUI})(\overline{DVI})$	
B 050	101	Req. Storage		
	37	Set Adder → P	$\overline{RAO}$	Update Address for next RNI
	41	Set Adder → Y	$\overline{RAO}$	
100	37	Adder → P		
	41	Adder → Y		
	51	X → Addend	$(\overline{ADQ})(\overline{DVI})(\overline{MUI})$	
	49	A → Adder	ADD+AND+EOR+SUB+DVI+MUI	
150	9	Set RNI	$\overline{RAO}$	
RNI				
B 250	31	Set Adder → A	(LDA+ADD+AND+EOR+SUB)(RNI)	
300	31	Adder → A		
	9	Clr. ROP	RNI+STO	
		Wait for reply		

CODE	INSTRUCTION	FUNCTION
AND-A	AND with A	A ANDed with (E.A.) to A

SEQUENCE / CYCLE(S):

EXECUTION TIME: ROP

TIME		PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR					
B	050	101	Req. Storage		
B	150	9	Set ROP	(End ADR)$\overline{(STA+JMP+STQ+SPA+RTJ)}$	
B	300	9	Clr. ADR	RNI+ROP	
			Wait for reply		
A	000	39	Z → X		
ROP					
A	100	51	X → Addend		
	300	49	+1 → Adder	$(\overline{EXI})(\overline{DVI})(\overline{MUI})$	
		51	P → Adder	$(\overline{EXI})(\overline{DVI})(\overline{MUI})$	
B	050	101	Req. Storage		
		37	Set Adder → P	$\overline{RAO}$	Update Address for next RNI
		41	Set Adder → Y	$\overline{RAO}$	
	100	37	Adder → P		
		41	Adder → Y		
		51	X → Addend	$(\overline{ADQ})(\overline{MUI})(\overline{DVI})$	
		49	A → Adder	ADD+AND+SUB+MUI+DVI	Forms logical product of (A) and (E.A.)
		45	Set L.P.	AND	
	150	9	Set RNI	$\overline{RAO}$	
RNI					
B	250	31	Set Adder → A	LDA+ADD+AND+EOR+SUB	
	300	31	Adder → A		
		9	Clr. ROP	RNI+STO	
		45	Clr. L.P.		
			Wait		

CODE	INSTRUCTION	FUNCTION
EOR-B	Exclusive OR	A ORed with (E.A.) to A

SEQUENCE / CYCLE(S): ROP

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
B 050	101	Req. Storage		
B 150	9	Set ROP	(End ADR)($\overline{STA+JMP+STQ+SPA+RTJ}$)	
B 300	9	Clr. ADR	RNI+ROP+STO	
		Wait		
A 000	39	Z → X		
ROP				
A 100	51	X → Addend		
A 300	49	+1 → Adder	($\overline{EXI}$)($\overline{MUI}$)($\overline{DVI}$)	
	51	P → Adder	($\overline{EXI}$)($\overline{MUI}$)($\overline{DVI}$)	
B 050	101	Req. Storage		
	37	Set Adder → P	$\overline{RAO}$	Update Address for next RNI
	41	Set Adder → Y	$\overline{RAO}$	
100	37	Adder → P		
	41	Adder → Y		
	51	X → Addend	($\overline{ADQ}$)($\overline{DVI}$)($\overline{MUI}$)	
	49	A → Adder	ADD+AND+EOR+SUB+MUI+DVI	forms logical difference of (A) and (E.A.)
	45	Set XR	EOR+(MUI+DVI)SRI	
150	9	Set RNI	$\overline{RAO}$	
RNI				
B 250	31	Set Adder → A	LDA+ADD+AND+EOR+SUB	
300	31	Adder → A		
	45	Clr. XR		
	9	Clr. ROP	RNI+STO	
		Wait		

CODE	INSTRUCTION	FUNCTION
LDA-C	Load A	(E.A.) to A

SEQUENCE / CYCLE(S):

ROP

EXECUTION TIME :

TIME		PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR					
B	050	101	Req. Storage		
B	150	9	Set ROP	(End ADR)$\overline{(STA+JMP+STQ+SPA+RTJ)}$	
B	300	9	Clr. ADR	RNI+ROP+STO	
			Wait		
A	000	39	Z → X		
ROP					
A	100	51	X → Addend		Not used, adder is not gated out (used for complementing on other instructions)
A	300	49	+1 → Adder	$\overline{EXI}\,\overline{MUI}\,\overline{DVI}$	Update Address for next RNI
		51	P → Adder	$\overline{EXI}\,\overline{MUI}\,\overline{DVI}$	
B	050	101	Req. Storage		
		37	Set Adder → P	$\overline{RAO}$	
		41	Set Adder → Y	RAO	
	100	37	Adder → P		
		41	Adder → Y		
		51	X → Addend	$\overline{ADQ}\,\overline{MUI}\,\overline{DVI}$	
			Augend = all ones		(E.A.) pass straight through the Adder
	150	9	Set RNI	$\overline{RAO}$	
RNI					
B	250	31	Set Adder → A	LDA+ADD+AND+EOR+SUB	
	300	31	Adder → A		
		9	Clr. ROP	RNI+STO	
	375		Wait		

CODE	INSTRUCTION	FUNCTION
RAO-D	Replace Add one	(E.A.+1) to E.A.

SEQUENCE / CYCLE(S): ROP

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
B 050	101	Req. Storage		
B 150	9	Set ROP	(End ADR)$(\overline{STA+JMP+STQ+SPA+RTJ})$	
B 300	9	Clr. ADR	RNI+ROP+STO	
		Wait		
A 000	39	Z → X		(E.A.) → X
ROP				
A 100	51	X → Addend		
	51	P → Adder	$\overline{EXI+MUI+DVI}$	Not used
	49	+1 → Adder	$(\overline{EXI+MUI+DVI})$	Not used
B 050	101	Req. Storage		
100	51	X → Addend	$(\overline{ADQ})(\overline{MUI})(\overline{DVI})$	
	49	+1 → Adder	RAO	
B 150	9	Set STO	RAO	
B 200				
250	39	Set Adder → X	STO	
B 300	9	Clr. ROP	STO+RNI	
	39	Adder → X		(E.A.) + 1 → X
375		Wait		

CODE	INSTRUCTION	FUNCTION
RAO-D	Replace Add one	

SEQUENCE / CYCLE(S): STO

EXECUTION TIME :

TIME		PAGE / TERM	COMMAND	CONDITION	REMARKS
STO					
A	300	49	+1 → Adder	(STO)(A cycle)($\overline{\text{Blk.+1}}$)	
		51	P → Adder	(STO)(A cycle)	
B	050	101	Req. Storage		
		41	Set Adder → Y	(STO)(B cycle)	Update Address for next RNI
		37	Set Adder → P	(STO)(B cycle)	
	100	37	Adder → P		
		41	Adder → Y		
	150	9	Set RNI	(STO 2)	
RNI					
	300	9	Clr. STO	RNI	
	375		Wait		

CODE	INSTRUCTION	FUNCTION
LDQ-E	Load Q	(E.A.) to Q

SEQUENCE / CYCLE(S): ROP

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
B 050	101	Req. Storage		
B 150	9	Set ROP	(End ADR)$\overline{(STA+JMP+STQ+SPA+RTJ)}$	
B 300	9	Clr. ADR	RNI+ROP+STO	
		Wait		
A 000	39	Z → X		
ROP				
A 100	51	X → Addend		Not used
A 300	49	+1 → Adder	$(\overline{EXI})(\overline{DVI})(\overline{MUI})$	
	51	P → Adder	$(\overline{EXI})(\overline{DVI})(\overline{MUI})$	
B 050	101	Req. Storage		
	37	Set Adder → P	$\overline{RAO}$	Update Address for next RNI
	41	Set Adder → Y	$\overline{RAO}$	
100	37	Adder → P		
	41	Adder → Y		
	51	X → Addend	$(\overline{ADQ})(\overline{MUI})(\overline{DVI})$	
150	9	Set RNI	$\overline{RAO}$	
RNI				
B 250	33	Set Adder → Q	(LDA+ADQ)RNI	(E.A.) → Q
300	33	Adder → Q		
	9	Clr. ROP	RNI+STO	
		Wait		

CODE	INSTRUCTION	FUNCTION
ADQ-F	Add to Q	(E.A.) + Q to Q

SEQUENCE / CYCLE(S): ROP

EXECUTION TIME :

TIME		PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR					
B	050	101	Req. Storage		
B	150	9	Set ROP	(End ADR)($\overline{STA+JMP+STQ+SPA+RTJ}$)	
B	300	9	Clr. ADR	RNI+ROP+STO	
			Wait		
A	000	39	Z → X		
ROP					
A	100	51	X → Addend		Not used
A	300	49	+1 → Adder	($\overline{EXI}$)($\overline{MUI}$)($\overline{DVI}$)	
		51	P → Adder	($\overline{EXI}$)($\overline{MUI}$)($\overline{DVI}$)	
B	050	101	Req. Storage		
		37	Set Adder → P	$\overline{RAO}$	Update Address for next RNI
		41	Set Adder → Y	$\overline{RAO}$	
	100	37	Adder → P		
		41	Adder → Y		
		49	X → Augend	ADQ	
		51	Q → Adder	ADQ	
	150	9	Set RNI	$\overline{RAO}$	(E.A.) +(Q) → Q
RNI					
B	250	33	Set Adder → Q	(LDQ+ADQ)RNI	
	300	33	Adder → Q		
		9	Clr. ROP	RNI+STO	
			Wait		

CODE	INSTRUCTION	FUNCTION
		Interrupt occurs during first pass of Addressing

SEQUENCE / CYCLE(S):

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
A 050	71	Set INT REG.		
ADR 100				
250	69	Set INT F.F.	(INT)(Enabled)(RNI+(Ind) Adr.)	
300	49	+1 → Adder	INT	
	45	Set XR	INT	
	49	Y → Adder	$(\overline{INT})(\overline{ind})(q)(RNI+\Delta\neq 0)$	Not used
	51	Q → Adder	$(\overline{INT})(\overline{ind})(q)(RNI+\Delta\neq 0)$	
	13	Set Read Index	$(\overline{INT})(\overline{ind})(i)(RNI+\Delta\neq 0)$	
350	23	Clr. F REG		
B 050	101	Req. Storage		
	39	Set Adder → X	$(\overline{ind})(q)(RNI+\Delta\neq 0)$+INT	
	41	Set state → Y	INT	
	41	Set Adder → Y	$(\overline{INT})(\overline{ind})(q)(RNI+\Delta\neq 0)$	Not used
100	39	Adder → X		(X) now = -1
	41	state → Y		
	51	P → Adder	INT+RTJ	(P)+(-1) → Adder
	49	X → Augend	INT(Δ=0)	
150	9	Set STO	(STA+STQ+SPA+RTJ)End ADR+INT	
STO				
B 250	39	Set Adder → X	$\overline{RAO}$	(X) now = original (P)
300	9	Clr. ADR	RNI+ROP+STO	
		Wait		

(Continued on page 121.)

CODE	INSTRUCTION	FUNCTION
		Interrupt occurs during Indirect Addressing

SEQUENCE / CYCLE(S):

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
ADR				
A 050	71	Set INT REG.		
100	51	X → Addend	$\overline{RNI(\Delta=0)}$	
	23	Clr. ind	$X_{15}=0(RNI + r)$	
250	41	Set Adder → Y		
	69	Set INT F.F.	(INT)(Enabled)(ind+RNI)	
300	49	+1 → Adder	INT	
	45	Set XR	INT	
350	23	Clr. F REG	INT	
B 050	101	Req. Storage		
	39	Set Adder → X	$(\overline{ind})(q)(RNI+\Delta\neq 0)$+INT	
	41	Set state → Y	INT	
100	39	Adder → X		(X) now = -1
	41	State → Y		
	51	P → Adder	INT+RTJ	} (P)+(-1) → Adder
	49	X → Augend	INT(Δ=0)	
150	9	Set STO	(STA+STQ+SPA+RTJ)End ADR+INT	
STO				
B 250	39	Set Adder → X	$\overline{RAO}$	(X) now = original (P)
300	9	Clr. ADR	RNI+STO+ROP	

(Continued on page 121.)

CODE	INSTRUCTION	FUNCTION
		Interrupt occurs during REG inst.

SEQUENCE / CYCLE(S):

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
A 050	71	Set INT REG.		
REG				
A 100				
250	69	Set INT F.F.	(INT)(Enabled)(RNI+(ind)ADR)	
300	51	P → Adder	Shift cycle	
	49	+1 → Adder	Shift cycle	
B 050	101	Req. Storage		
	41	Set state → Y	INT	
	41	Set Adder → Y	EXI+SPB+CPB+INT	Not used - used only in returning to RNI
	37	Set Adder → P	EXI+SPB+CPB	
B 100	41	state → Y		(Y) = location of return Address
	37	Adder → P		return Address → P
	51	P → Adder	(INT+RTJ)(ADR+REG)	
150	9	Set RNI	EXI+SPB+CPB+INT	Not used
	9	Set ROP	(SPB+CPB+EXI)(INT)	Not used
STO	9	Set STO	[(STA+STQ+SPA+RTJ)End ADR+INT]ADR+REG	
250	39	Set Adder → X	RAO	
300	39	Adder → X		(X) = return Address which is stored during STO
	9	Clr. REG		

(Continued on page 121.)

CODE	INSTRUCTION	FUNCTION
		Interrupt

SEQUENCE / CYCLE(S): STO

EXECUTION TIME :

TIME	PAGE / TERM	COMMAND	CONDITION	REMARKS
STO				
A 100	49	Y → Adder	INT+RTJ	location of return Address → Adder
300	69	Clr. Enable INT		
	69	Clr. INT F.F.		
A 250	37	Set Adder → P	INT+RTJ	
A 300	37	Adder → P		
	51	P → Adder		
	49	+1 → Adder		
B 050	101	Req. Storage		
	37	Set Adder → P		location of return Address + 1 → P, Y
	41	Set Adder → Y		
100	37	Adder → P		
	41	Adder → Y		
150	9	Set RNI		
300	9	Clr. STO	RNI	

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